Post-trial Motions Hearing

SAMSUNG'S MOTION FOR JMOL ON WILLFULNESS (DKT. 580)

KAIST IP US OPPOSITION (DKT. 594)

SAMSUNG'S REPLY (DKT. 603)

KAIST IP US SURREPLY (DKT. 620)

Copying and Recklessness

2002 – 2003

- T.S. Park knew of Korean application
  Dkt. 494 (6/13/18 PM), at 41:10-12; see also Dkt. 547-7 at 9:13-23
- Kinam Kim (CEO) & Donggun Park (VP) aware of patent filing
  Dkt. 488 (6/11/18 PM), at 97:14-21 (citing PX2068), 98:21-99:15 (citing PX1374)
  PX2068 (Kinam Kim email); PX1374 (Donggun Park email)
- ***Prof. Lee asks Samsung to license***
  Dkt. 488 (6/11/18 PM), at 97:5-13

2006

- Samsung invites Prof. Lee to lecture its engineers
  Dkt. 488 (6/11/18 PM), at 100:20-101:2

2011 – 2012

- **P*&IB asks Samsung to license***
  Dkt. 489 (6/12/18 AM), at 29:11-15
- Samsung invites Prof. Lee to lecture its engineers
  Dkt. 488 (6/11/18 PM), at 102:6-15, 103:16-20; PX1377 (D.W. Kim email)
- Samsung engineers at lawyers instruction review patent
  Dkt. 493 (6/13/18 AM), at 65:21-66:4
- Dongwon Kim reads the patent – does not tell superiors
  Dkt. 494 (6/13/18 PM), at 6:2-15

2013 – 2015

- 14nm still in development
  Dkt. 494 (6/13/18 PM), at 7:17-8:8; Dkt. 493 (6/13/18 AM), at 48:20-23
- ***P&IB again asks Samsung to license***
  Dkt. 488 (6/11/18 PM) at 99:18-22
- Date of first infringement
  Dkt. 491 (6/12/18 PM), at 212:25-213:3; Dkt. 497 (6/14/18 PM), at 108:14-16

Copying

Copying "Technology" Is Willful

"Marvell's engineers duplicated the technology described in Dr. Kavcic and Dr. Moura's papers . . . [T]he papers are virtually identical to what is described in the patents . . . Marvel's only responses to this robust evidence are that it did not adopt the detailed algorithm laid out in the CMU papers and the written description of the CMU patents and that it obtained its own later patents for . . . a sub-optimal version of Kavcic's detector. Neither response undermines the foregoing evidence."

Carnegie Mellon Univ. v. Marvell Tech. Gp., Ltd., 807 F.3d 1283, 1300 (Fed. Cir. 2015) (internal citations, quotations omitted)

Expert Testimony on Copying

Dr. Kuhn:

Q. And what is that evidence?

A. Well, there's a series of presentations that Professor Lee gave to Samsung, and you've heard some discussion on that already. There's two groups of presentations, a 2006 and a 2012 group. And I'm going to be showing some slides, particularly from the 2006 group, that show key features of Professor Lee's design that have been transferred to Samsung through these presentations.

Dkt. 491, June 12, 2018 PM Trial Tr. at 18:10-20

Q. . . . So based on the evidence that you've seen, where does the Samsung design come from?

A. All the evidence I've seen suggests it came from Professor Lee.

Dkt. 491 (6/12/18 PM) at 20:25-22:1

Dr. Subramanian:

Q. You did no investigation whatsoever as to whether the Defendants in this case copied the '055 patent, fair point?

A. Yes. I did not testify to that.

…

Q. Are there any other independent experts in this case trained in technical matters other than you?

A. Well, there are. I mean, Dr. Wallace, he did not address copying either, to my understanding.

Dkt. 497, June 14, 2018 PM Trial Tr. at 31:7-25

Prof. Lee's Design Taken to Samsung Engineers

Q. After you worked with Professor Lee to build the bulk silicon FinFET at Seoul National University, you discussed the design with your colleagues at Samsung, correct?
A. Yes, I would believe that I did.
Q. You shared with Samsung the concept of the Fin being connected to the bulk silicon substrate, correct?
A. Yes, I did.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 40:20-41:1 (T. Park cross)

Q. In 2011, you made the semiconductor R&D center aware of Professor Lee's '055 patent, correct?
A. Yes.
Q. What engineers in Samsung's semiconductor R&D center did you review the '055 patent with?
A. It was a group of engineers who worked on future process technologies within Samsung's Semiconductor R&D center.

Dkt. 493, June 13, 2018 AM Trial Tr. at 65:21-61:4 (Jong-Soo Seo);
see also Dkt. 547-12 at 12:22-24, 13:7-11 (same)

Samsung Engineers Read Prof. Lee's Korean Patent and Publications

Q. You were aware of Professor Lee's Korean patent application as early as September 2002, correct?

A. That's right, I was.

Dkt. 494, June 13, 2018 PM Trial Tr. at 41:10-12 (T. Park cross)

Q. Now, you read research that Professor Lee performed relating to bulk FinFET technology, correct?

A. **Yes, I read his paper**. And there was an occasion that I read his paper.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 4:24-5:2 (cross)

Samsung Points To 2003 IEDM Article

SAMSUNG
NEWSROOM

Press Resources > Press Release

Samsung Announces Mass Production of Industry's

compared to Samsung's 20nm process technology, this newest process enables up to 20 percent faster speed, 35 percent less power consumption and 30 percent productivity gain.

This ground-breaking accomplishment is a result of Samsung's unparalleled R&D efforts in FinFET technology since the early 2000s. Starting with a research article presented at IEDM (International Electron Devices Meeting) in 2003, Samsung has continuously made progress and announced its technological achievements in FinFET research and has also filed a pool of key patents in the field.

SAMSUNG TOMORROW

"Samsung's advanced 14nm **FinFET process technology** is undoubtedly the most advanced logic process technology in the industry," said Gabsoo Han, Executive Vice President of Sales & Marketing, System LSI Business, Samsung Electronics. "We expect the production of our 14nm mobile application processor to positively impact the growth of the mobile industry by enabling further performance improvements for cutting-edge smartphones."

KAIST IP US LLC, v. SAMSUNG
PX1197
Case No. 2:16-CV-01314-JRG-RSP

https://news.samsung.com/global/samsung-announces-mass-production-of-industrys-first-14nm-finfet-mobile-application-processor 1/3

technology, Samsung has strengthened its leadership in 3D semiconductors in both memory and logic semiconductors that addresses the current scaling limitations with planar designs.

Samsung's leading-edge14nm FinFET process will be adopted by its Exynos 7 Octa, then expanded to other products throughout the year.

TAGS *14nm FinFET, Announces, Mobile Application Processor, Samsung* SHARE

For any issues related to customer service, please go to samsung.com/contactus for assistance.
For media inquiries, please contact hq.comm@samsung.com.

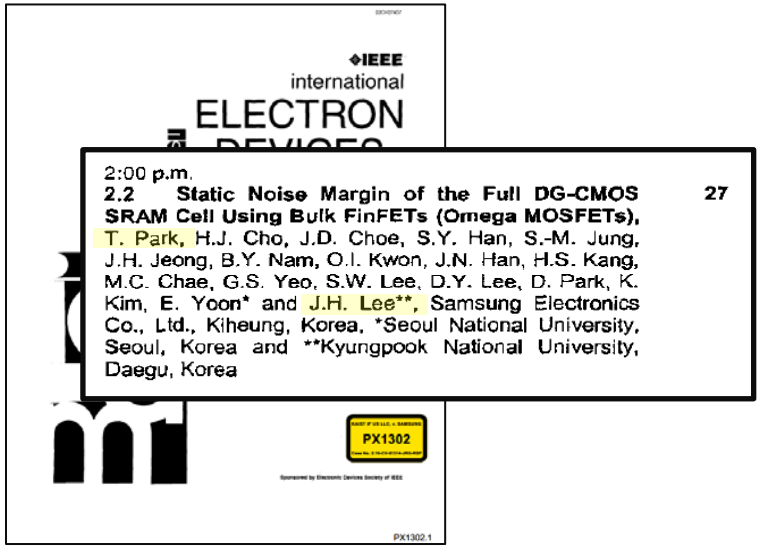
https://news.samsung.com/global/samsung-announces-mass-production-of-industrys-first-14nm-finfet-mobile-application-processor 2/3

2003 IEDM Article ➔ Prof. Lee's Omega Design

Q. And I want to turn to a passage in that document. I believe it's on Page 2. It says: This groundbreaking accomplishment is a result of Samsung's unparalleled R&D efforts in FinFET technology since the early 2000s, starting with the research article presented at IEDM, International Electron Device Meeting in 2003. Do you have knowledge as to whether a bulk FinFET transistor paper was published in 2003 at the IEDM Conference that named Samsung as authors?

A. I am aware.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 104:19-105:8 (Prof. Lee)


IEEE international ELECTRON DEVICES

2:00 p.m.
2.2 **Static Noise Margin of the Full DG-CMOS SRAM Cell Using Bulk FinFETs (Omega MOSFETs),** 27
T. Park, H.J. Cho, J.D. Choe, S.Y. Han, S.-M. Jung, J.H. Jeong, B.Y. Nam, O.I. Kwon, J.N. Han, H.S. Kang, M.C. Chae, G.S. Yeo, S.W. Lee, D.Y. Lee, D. Park, K. Kim, E. Yoon* and J.H. Lee**, Samsung Electronics Co., Ltd., Kiheung, Korea, *Seoul National University, Seoul, Korea and **Kyungpook National University, Daegu, Korea

PX1302

PX1302.1

Q. So I want to do two things. First, can you examine static -- can you pull up the title? It says: Bulk FinFET Omega MOSFETs. Do you see that, sir?

A. Yes, I see it.

Q. And is that the name that's used in the industry for your '055 patent design?

A. Yes.

Q. Who's the senior author on this article?

A. I am.

Q. So in 2015, Samsung issued a press release announcing the commercialization of bulk FinFET technology.

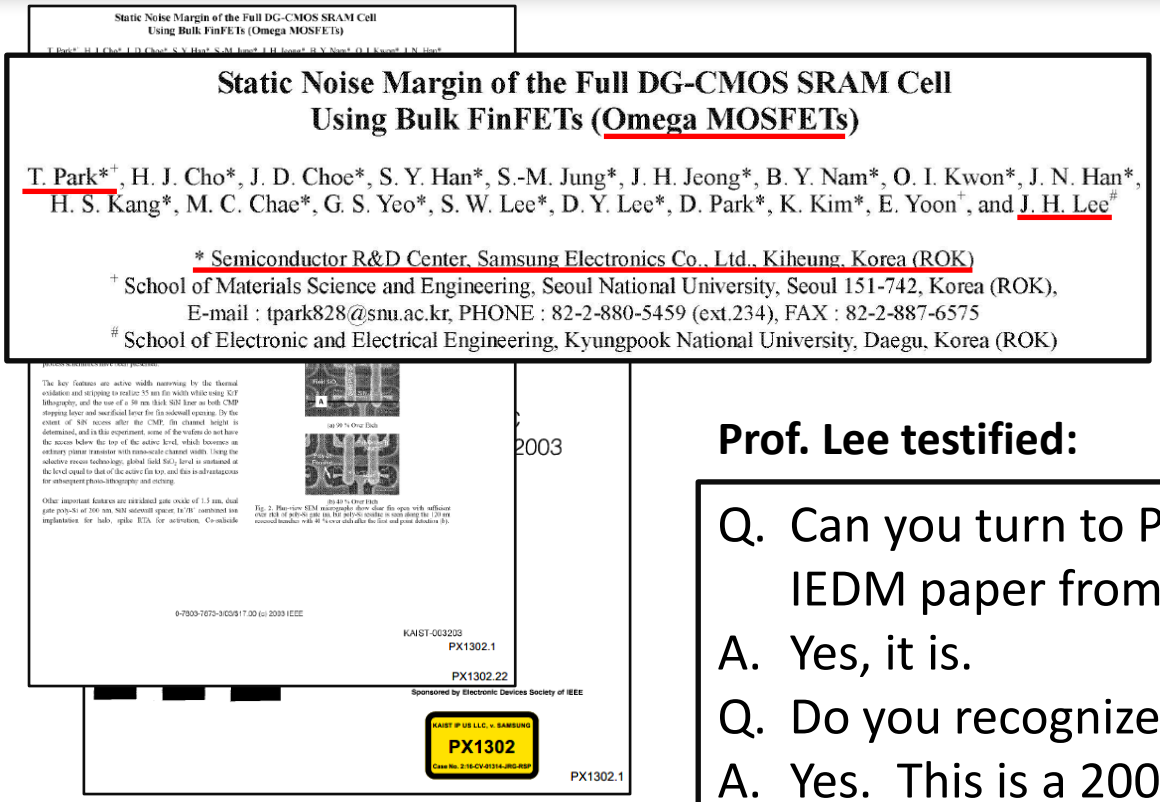
A. Yes. And the IEDM paper that Samsung points to in the press release is this paper.

Q. It's the paper on Omega bulk MOSFETs that you're the senior author on?

A. Correct.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 105:17-106:8 (Prof. Lee)

Prof. Lee's Omega Design = Patented Invention



Static Noise Margin of the Full DG-CMOS SRAM Cell
Using Bulk FinFETs (Omega MOSFETs)

T. Park*+, H. J. Cho*, J. D. Choe*, S. Y. Han*, S.-M. Jung*, J. H. Jeong*, B. Y. Nam*, O. I. Kwon*, J. N. Han*, H. S. Kang*, M. C. Chae*, G. S. Yeo*, S. W. Lee*, D. Y. Lee*, D. Park*, K. Kim*, E. Yoon+, and J. H. Lee#

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2003

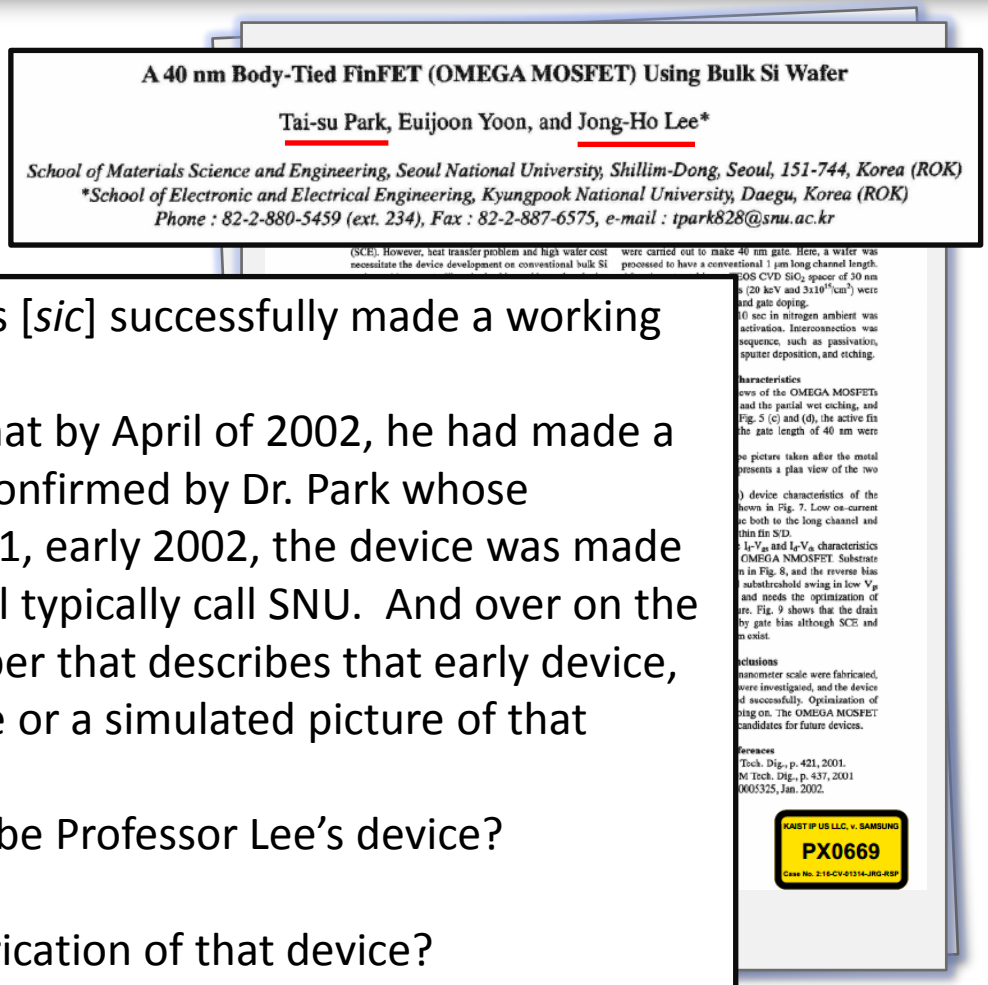
KAIST-003203
PX1302.1
PX1302.22
Sponsored by Electronic Devices Society of IEEE
KAIST IP US LLC, v. SAMSUNG
PX1302
PX1302.1

Prof. Lee testified:

Q. Can you turn to PX-1302. Is this the -- an IEDM paper from 2003?
A. Yes, it is.
Q. Do you recognize this document?
A. Yes. This is a 2003 IEDM paper that I wrote with Samsung. So this is a joint publication between Samsung and me in 2003. And a copy of my design, which is stated in my patent specification, is implemented here.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 105:9-16

Published Design Practices' 055 Patent


A 40 nm Body-Tied FinFET (OMEGA MOSFET) Using Bulk Si Wafer

Tai-su Park, Euijoon Yoon, and Jong-Ho Lee*

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Q. Now, are you aware that Professor Lee's [*sic*] successfully made a working version of his invention*?*

A. Yes. I understand from Professor Lee that by April of 2002, he had made a working version of this device. That's confirmed by Dr. Park whose testimony says between the end of 2001, early 2002, the device was made at Seoul National University, which we'll typically call SNU. And over on the right-hand side here in PX-0669 is a paper that describes that early device, and you can see a picture of that device or a simulated picture of that device in the paper.

Q. Now, does this -- does this paper describe Professor Lee's device?

A. Yes.

Q. And does it describe the successful fabrication of that device?

A. Yes.

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 65:11-66:2 (Dr. Kuhn)

Published Design Practices' 055 Patent

Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers

T. Park*†, S. Choi*, D. H. Lee*, J. R. Yoo*, B. C. Lee*, J. Y. Kim*, C. G. Lee*, K. K. Chi*, S. H. Hong*, S. J. Hyun*, Y. G. Shin*, J. N. Han*, I. S. Park*, U I. Chung*, J. T. Moon*, E. Yoon†, and J. H. Lee#
* Semiconductor R&D Center, Samsung Electronics Co., Ltd., Kiheung, Korea
† School of Materials Science and Engineering, Seoul National University, Seoul, Korea
# School of Electronic and Electrical Engineering, Kyungpook National University, Daegu, Korea

Q. Now, are you aware of any other later attempts to make Professor Lee's invention?

A. Yes. I understood Samsung followed up with its own fabrication. Again, I cite Dr. Park from Samsung. And that particular device, which I'm going to call the VLSI device to distinguish it from the other one, was completed after July of 2002. And a paper representing that device is PX-0191. We've seen this paper before. I'm going to call this the VLSI 2003 paper.

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 66:12-22 (Dr. Kuhn)

Q. And in this paper, both Samsung and Professor Lee are calling his invention the body-tied FinFET?

A. That's correct. Or the alternative name of Omega MOSFET.

Dkt. 489, **June 12, 2018 AM Trial Tr.** at 67:13-16 (Dr. Kuhn)

PX0191

KAIST-019584

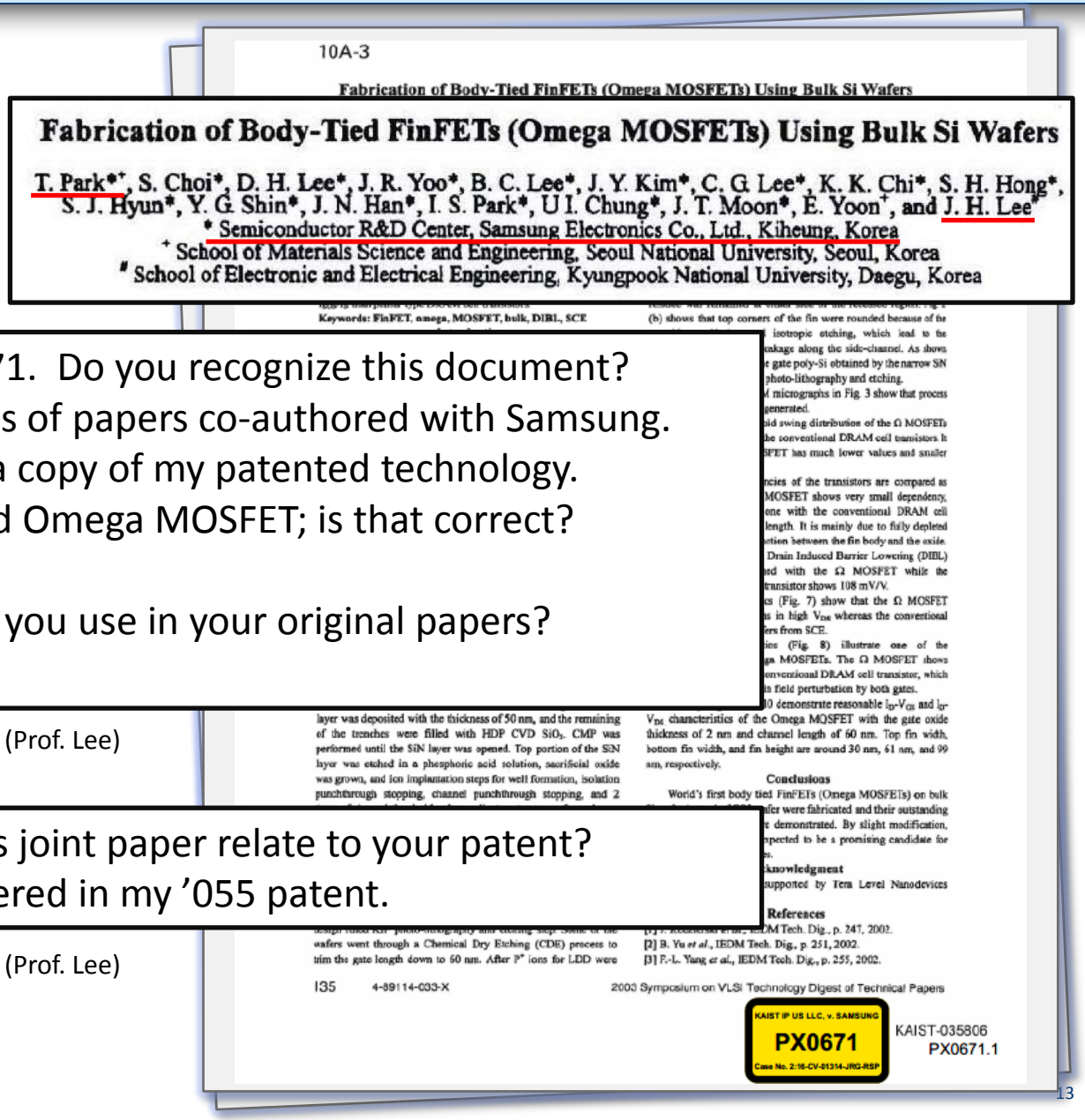
Published Design Practices' '055 Patent

Q. I now want to look at PX 671. Do you recognize this document?
A. Yes. This is a first of a series of papers co-authored with Samsung. And here Samsung makes a copy of my patented technology.
Q. The title is -- says Body-Tied Omega MOSFET; is that correct?
A. Correct.
Q. Is this the same as the title you use in your original papers?
A. Correct.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 93:15-25 (Prof. Lee)

Q. How does the design in this joint paper relate to your patent?
A. It is one of the designs covered in my '055 patent.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 95:10-12 (Prof. Lee)



10A-3

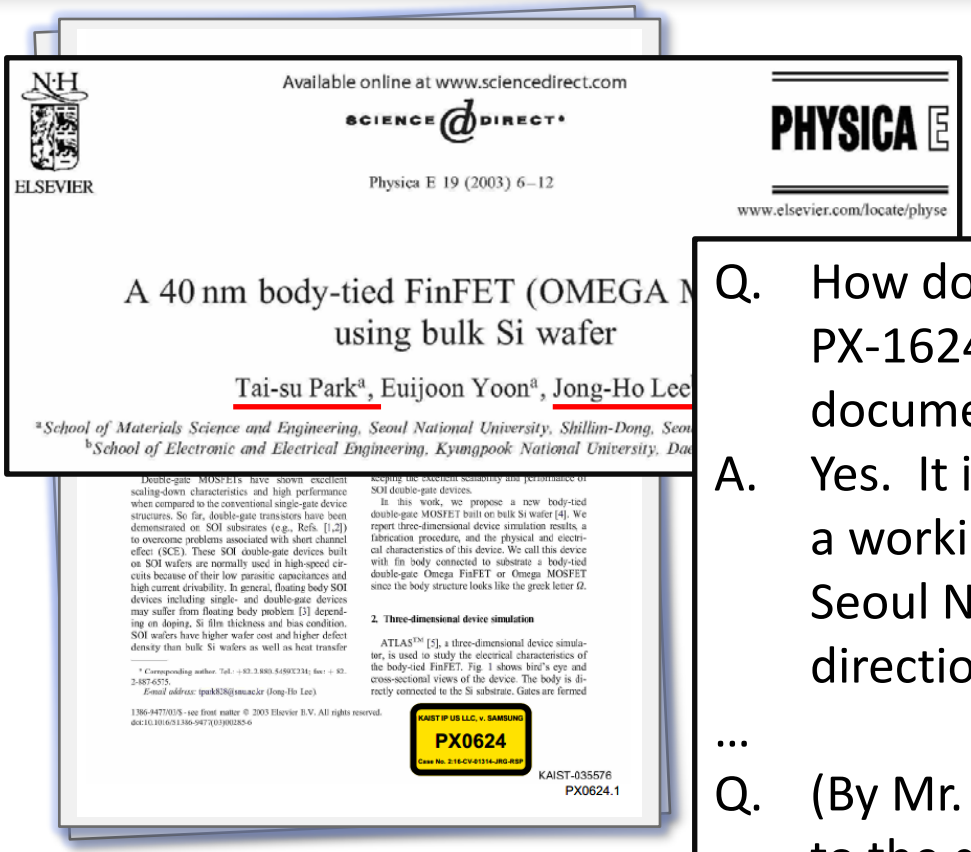
Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers

Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers

T. Park*†, S. Choi*, D. H. Lee*, J. R. Yoo*, B. C. Lee*, J. Y. Kim*, C. G. Lee*, K. K. Chi*, S. H. Hong*, S. J. Hyun*, Y. G. Shin*, J. N. Han*, I. S. Park*, U I. Chung*, J. T. Moon*, E. Yoon†, and J. H. Lee#
* Semiconductor R&D Center, Samsung Electronics Co., Ltd., Kiheung, Korea
† School of Materials Science and Engineering, Seoul National University, Seoul, Korea
# School of Electronic and Electrical Engineering, Kyungpook National University, Daegu, Korea

Keywords: FinFET, omega, MOSFET, bulk, DIBL, SCE

Published Design Practices' 055 Patent



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Physica E 19 (2003) 6–12

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ELSEVIER

A 40 nm body-tied FinFET (OMEGA M
using bulk Si wafer

Tai-su Park[a], Euijoon Yoon[a], Jong-Ho Lee

[a]School of Materials Science and Engineering, Seoul National University, Shillim-Dong, Seo
[b]School of Electronic and Electrical Engineering, Kyungpook National University, Da

Double-gate MOSFETs have shown excellent scaling-down characteristics and high performance when compared to the conventional single-gate device structures. So far, double-gate transistors have been demonstrated on SOI substrates (e.g., Refs. [1,2]) to overcome problems associated with short channel effect (SCE). These SOI double-gate devices built on SOI wafers are normally used in high-speed circuits because of their low parasitic capacitances and high current drivability. In general, floating body SOI devices including single- and double-gate devices may suffer from floating body problem [3] depending on doping, Si film thickness and bias condition. SOI wafers have higher wafer cost and higher defect density than bulk Si wafers as well as heat transfer

keeping the excellent scalability and performance of SOI double-gate devices.

In this work, we propose a new body-tied double-gate MOSFET built on bulk Si wafer [4]. We report three-dimensional device simulation results, a fabrication procedure, and the physical and electrical characteristics of this device. We call this device with fin body connected to substrate a body-tied double-gate Omega FinFET or Omega MOSFET since the body structure looks like the greek letter Ω.

2. Three-dimensional device simulation

ATLAS™ [5], a three-dimensional device simulator, is used to study the electrical characteristics of the body-tied FinFET. Fig. 1 shows bird's eye and cross-sectional views of the device. The body is directly connected to the Si substrate. Gates are formed

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doi:10.1016/S1386-9477(03)00285-6

KAIST IP US LLC, v. SAMSUNG
PX0624
Case No. 2:16-CV-01314-JRG-RSP

KAIST-035576
PX0624.1

Q. How does this -- how does this -- let's turn to PX-1624 (sic). Do you recognize this document?

A. Yes. It is a paper published on the bulk FinFET, a working bulk FinFET that was made the Seoul National University laboratory under my direction.

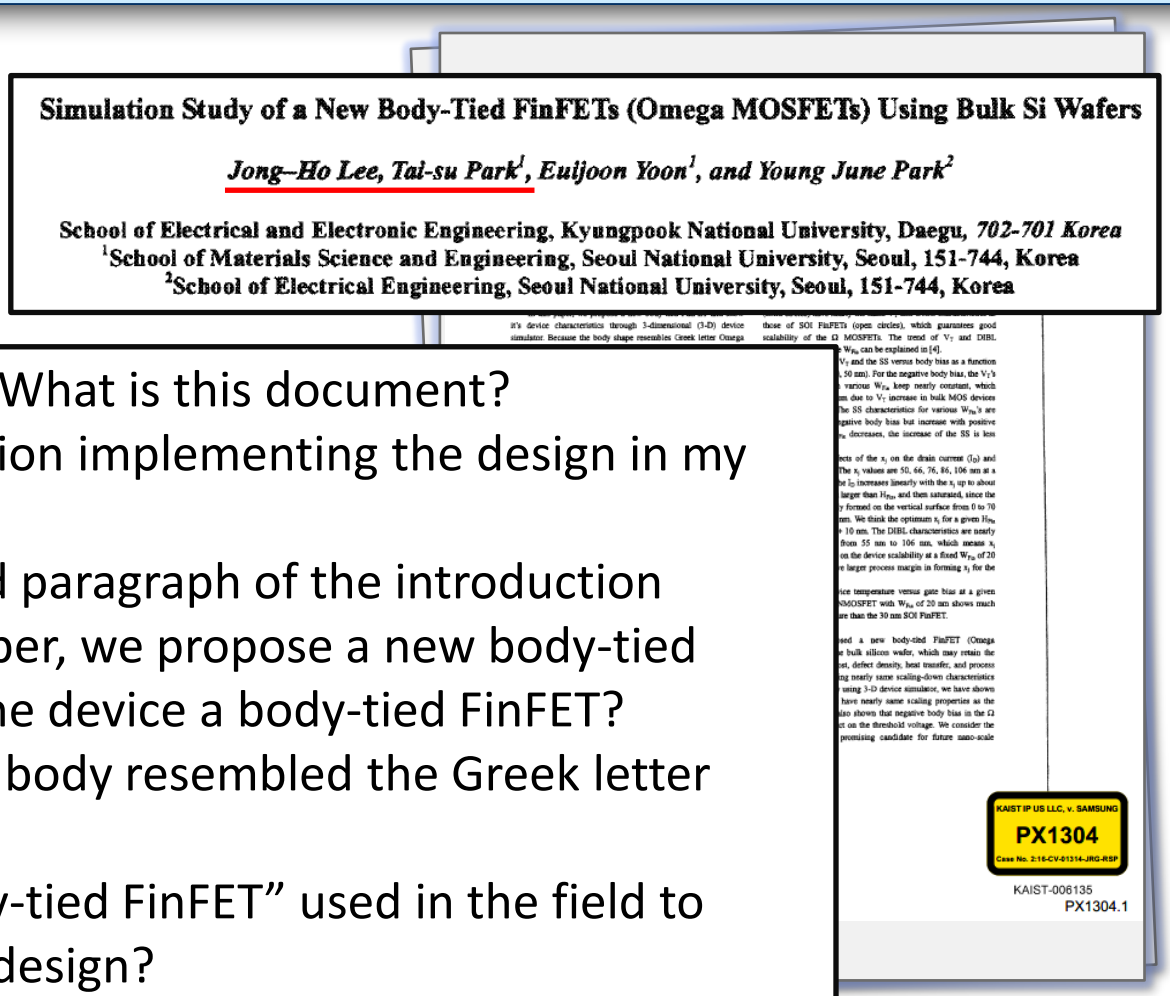
…

Q. (By Mr. Sheasby) How does this design relate to the designs described in your patent?

A. This paper implements one of the designs of my '055 patent.

Dkt. 488, **June 11, 2018 AM Trial Tr.** at 89:24-90:12 (Prof. Lee)

Published Design Practices' 055 Patent



Simulation Study of a New Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers

Jong–Ho Lee, Tai-su Park[1], Euijoon Yoon[1], and Young June Park[2]

School of Electrical and Electronic Engineering, Kyungpook National University, Daegu, *702-701 Korea*
[1]School of Materials Science and Engineering, Seoul National University, Seoul, 151-744, Korea
[2]School of Electrical Engineering, Seoul National University, Seoul, 151-744, Korea

KAIST IP US LLC, v. SAMSUNG
PX1304
Case No. 2:16-CV-01314-JRG-RSP

KAIST-006135
PX1304.1

Q. Can you turn to PX-1304? What is this document?

A. This is a paper of a simulation implementing the design in my '055 patent invention.

Q. Can you turn to the second paragraph of the introduction section? It says: In this paper, we propose a new body-tied FinFET. Why did you call the device a body-tied FinFET?

A. Because the outline of the body resembled the Greek letter Omega.

Q. Is the phrase "Omega body-tied FinFET" used in the field to describe your '055 patent design?

A. Yes.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 88:23-89:13 (Prof. Lee)

Evidence: Aware of Patent Filings

Available online at www.sciencedirect.com

A 40 nm body-tied FinFET (OMEGA MOSFET) using bulk Si wafer

Tai-su Park[a], Euijoon Yoon[a], Jong-Ho Lee[b,*]

[a] School of Materials Science and Engineering, Seoul National University, Shillim-Dong, Seoul 151-744, South Korea (ROK)
[b] School of Electronic and Electrical Engineering, Kyungpook National University, Daegu, South Korea (ROK)

Abstract

A new body-tied FinFET is proposed and fabricated on bulk Si wafer instead of SOI wafer. Three-dimensi... simulations show the characteristics of the proposed device and show that it can be implemented without deteri... channel effect. An active fin width of 25–40 nm and a gate length of 40 nm were realized by using sidewall spacer ...

PACS: 85.30.T; 85.40.V

Keywords: FinFET; Nano; MOSFET; DG-MOSFET; Body-tied; Bulk Si wafer

1. Introduction

Double-gate MOSFETs have shown excellent scaling-down characteristics and high performance when compared to the conventional single-gate device structures. So far, double-gate transistors have been demonstrated on SOI substrates (e.g., Refs. [1,2]) to overcome problems associated with short channel effect (SCE). These SOI double-gate devices built on SOI wafers are normally used in high-speed circuits because of their low parasitic capacitances and high current drivability. In general, floating body SOI devices including single- and double-gate devices may suffer from floating body problem [3] depending on doping, Si film thickness and bias condition. SOI wafers have higher wafer cost and higher defect density than bulk Si wafers as well as heat transfer issues. Thus, it is cost-effective and useful ... ment double-gate transistors on bulk Si w... keeping the excellent scalability and perfo... SOI double-gate devices.

In this work, we propose a new ... double-gate MOSFET built on bulk Si wafe... report three-dimensional device simulation ... fabrication procedure, and the physical a... cal characteristics of this device. We call t... with fin body connected to substrate a... double-gate Omega FinFET or Omega ... since the body structure looks like the ...

2. Three-dimensional device simulatio...

ATLAS™ [5], a three-dimensional d... tor, is used to study the electrical charact... the body-tied FinFET. Fig. 1 shows bird'... cross-sectional views of the device. The b... rectly connected to the Si substrate. Gates ...

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E-mail address: tpark828@snu.ac.kr (Jong-Ho Lee).

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doi:10.1016/S1386-9477(03)00285-6

KAIST IP US LLC, v. SAMSUNG
PX0624
Case No. 2:16-CV-01314-JRG-RSP

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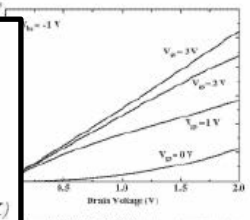
[1] J. Kedzierski, et al., Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation, International Electron Devices Meeting, Technical Digest, 2002, pp. 247–250.

[2] B. Yu, et al., FinFET scaling to 10 nm gate length, International Electron Devices Meeting, Technical Digest, 2002, pp. 251–254.

[3] Jean-Pierre Colinge, Silicon-on-Insulator Technology: Materials to VLSI, Kluwer Academic Publishers, Dordrecht, 1991.

[4] Jong-Ho Lee, Korean patent filed, File No. 10-2002-0005325, January 2002.

[5] Silvaco International Incorporated, ATLAS™ User's Manual, Version 5.2.0.R, 2000.



...annel OMEGA NMOS I_d–V_{ds} characteristics as ... gate bias.

possible floating body effect while keeping nearly the same short channel effect as in the SOI double-gate device. Body-tied double-gate devices were fabricated and characterized. The body-tied double-gate MOSFET is a very promising candidate for future devices.

Acknowledgements

This work was supported by Tera Level Nano-devices Project of MOST in 2002. TP and EY acknowledge the support of NRL Program of MOST.

References

[1] J. Kedzierski, et al., Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation, International Electron ... Technical Digest, 2002, pp. 247–250.
... FinFET scaling to 10 nm gate length, ...ctron Devices Meeting, Technical Digest, ...54.
...linge, Silicon-on-Insulator Technology: ...SI, Kluwer Academic Publishers, Dordrecht, ...
...nean patent filed, File No. 10-2002-0005325, ...
...nal Incorporated, ATLAS™ User's Manual, ...2000.

PX624 Practices '055 Patent

MR. SHEASBY: I want to turn to PX-1624 (sic), Page 5, Mr. Negrete, and I want to pull up Figure A.

Q. (By Mr. Sheasby) Can you describe what's being depicted in Figure A?

A. Figure A depicts a Fin that is connected to the substrate, and it becomes wider as it goes toward the substrate.

Q. Is the top rounded?

A. The top corners are rounded.

Q. So the original FinFET device that was made, the Fin was not rectangular. It widened as it went to the substrate and was rounded at top; is that correct?

A. Correct.

Q. In your patent, do you -- do you describe a technique called chamfering?

A. Yes.

Q. What is chamfering?

A. Chamfering is rounding the top corners of the Fin.

Q. In your patent, do you describe making the Fin wider as it approaches the substrate?

A. Yes.

Dkt. 488, **June 11, 2018 AM Trial Tr.** at 90:13-91:8 (Prof. Lee)

Lee Presentations

2006	First 2006 invitation from Samsung – email from Yong-Seok Lee Dkt. 488 (6/11/18 PM) at 100:2-10 (discussing PX1375) Dkt. 488, June 11, 2018 AM Trial Tr. at 89:24-90:12 (Prof. Lee) Dkt. 488, June 11, 2018 PM Trial Tr. at 88:23-89:1, 93:15-94:1-15, 95:10-12, 100:2-101:12 (Prof. Lee) Dkt. 489, June 12, 2018 AM Trial Tr. at 66:12-15, 66:20-22, 67:13-16 (Dr. Kuhn) Second 2006 invitation from Samsung Dkt. 488 (6/11/18 PM) at 100:20-101:2 "3-D MOSFETs for Nano-Scale CMOS Technology with Emphasis on DRAM Application" PX0899 (2006 presentation) at 9 (NanoMES paper, PX0669, and Physica E paper, PX0624), 10 (VLSI paper), 13, 27 (nonoverlapping gate), 20-21 (chamfering) "Bulk FinFETs for DRAM Application" PX1608 (2006 presentation), at 9 (NanoMES paper, PX0669, and Physica E paper, PX0624), 10 (VLSI paper), 19 (wall-shape fin and fin widening), 37 (nonoverlapping gate), 64 (chamfering)
2012	First 2012 invitation Samsung – email request from D.W. Kim Dkt. 488 (6/11/18 PM) at 102:6-15 (discussing PX1377) Dkt. 488, June 11, 2018 PM Trial Tr. at 102:6-15, 102:25-103:6, 103:7-103:24 (Prof. Lee) Second 2012 invitation from Samsung Dkt. 488 (6/11/18 PM) at 103:16-24 "Understanding of FinFETs" PX0878 at 24 (noting "Korea/USA patent"), 42 (source/drain junction depth), 46-47 (fin widening), 61 (quoting chamfering claim 15) "Bulk FinFETs for 14 nm Logic Technology Node: Critical Issues & Challenges" PX0856 at 6 (source/drain junction depth), 7 (wall-shape fin), 14 (chamfering), 19 (selective epitaxy), 20-26 (fin widening), 49-54 (contact resistance)

2006: Invited Prof. Lee Presentation

From: Lee Yong-seok [mailto:ys1407.lee@samsung.com]
Sent: Friday, February 10, 2006 9:47 AM
To: jongho@ee.knu.ac.kr
Subject: SEMICON KOREA 2006 Request for Material

Hello professor, how are you?

This is Lee Yong-seok who is in charge of the next generation products such as FinFET and CTF at the Semiconductor Memory Project Division at Samsung Electronics Co., Ltd.
I am sending you this mail for nothing else but to ask you a favor to send me PPT material on '3D MOSFETs for Nano-scale CMOS Technology'
that you presented at SEMICON KOREA 2006 on February 8.
It is to utilize in the analysis work to be proceeded in the future.
I also attended S3 and listened to your presentation...^^

Then have a good day now...
Please do me a favor...

KAIST IP US LLC, v. SAMSUNG
PX1375
Case No. 2:16-CV-01314-JRG-RSP

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 100:2-10 (Prof. Lee)

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KAIST IP US LLC, v. SAMSUNG
PX1375
Case No. 2:16-CV-01314-JRG-RSP

Mr. Sheasby: Let's pull up 1375.

Q. (By Mr. Sheasby) Do you recognize this document?
A. This is an email from a Samsung engineer. He is asking for my bulk FinFET presentation material.
Q. And this is dated February 2006; is that correct?
A. Correct.
Q. And he states he's in charge of next generation products such as FinFET?
A. Correct.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 100:2-10 (Prof. Lee)

Semicon Korea '06

3-D MOSFETs for Nano-Scale CMOS Technology with Emphasis on DRAM Application

Jong-Ho Lee

jongho@ee.knu.ac.kr
School of EECS and National Education Center for Semiconductor Technology
Kyungpook National University, Daegu, 702-701 Korea

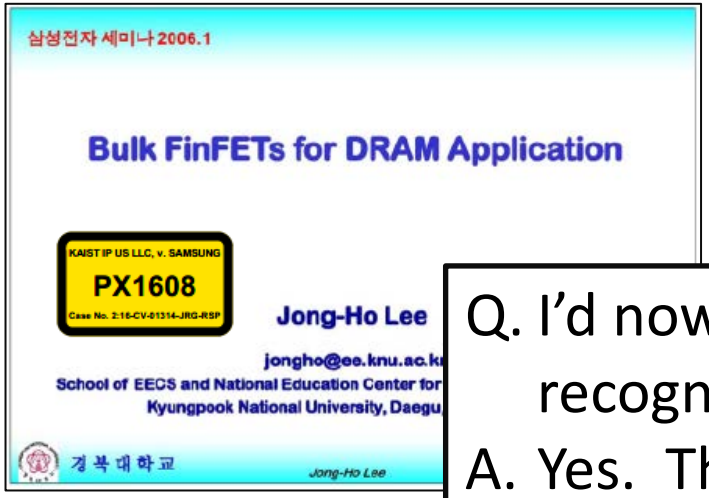
KAIST IP US LLC, v. SAMSUNG
PX0899

Nanosystems Lab. Jong-Ho Lee KYUNGPOOK NATIONAL UNIVERSITY

Q. And can you turn to PX-899 -- PX-899, please? Do you recognize this document?
A. This is the presentation that I sent to the Samsung researcher.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 100:11-14 (Prof. Lee)

2006: Invited Prof. Lee Presentation



Q. I'd now like to turn to PX-1608. Do you recognize this document?

A. Yes. This is a presentation material that I used when I provided a lecture after being invited from those at Samsung Electronics in 2006.

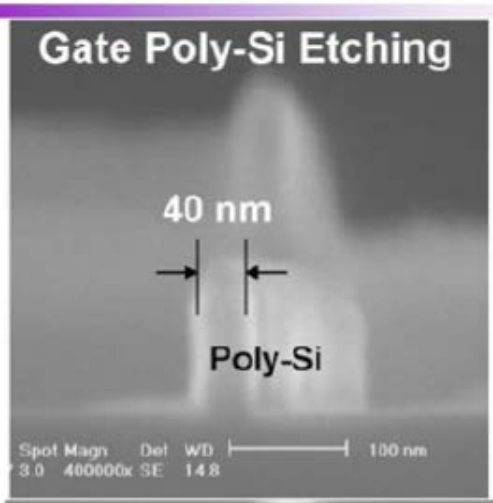
Q. Do you know who attended this presentation?

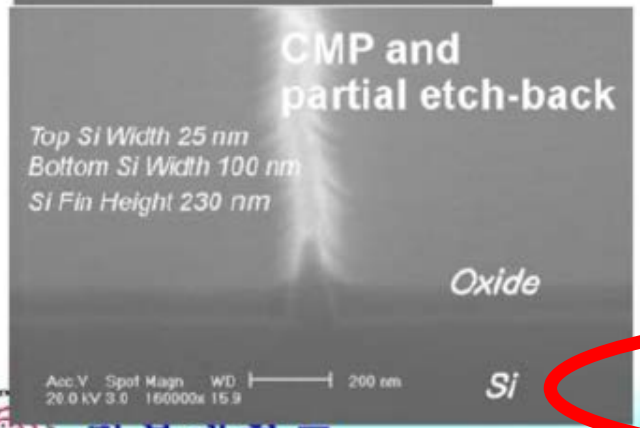
A. Many engineers working on various chips at Samsung participated.

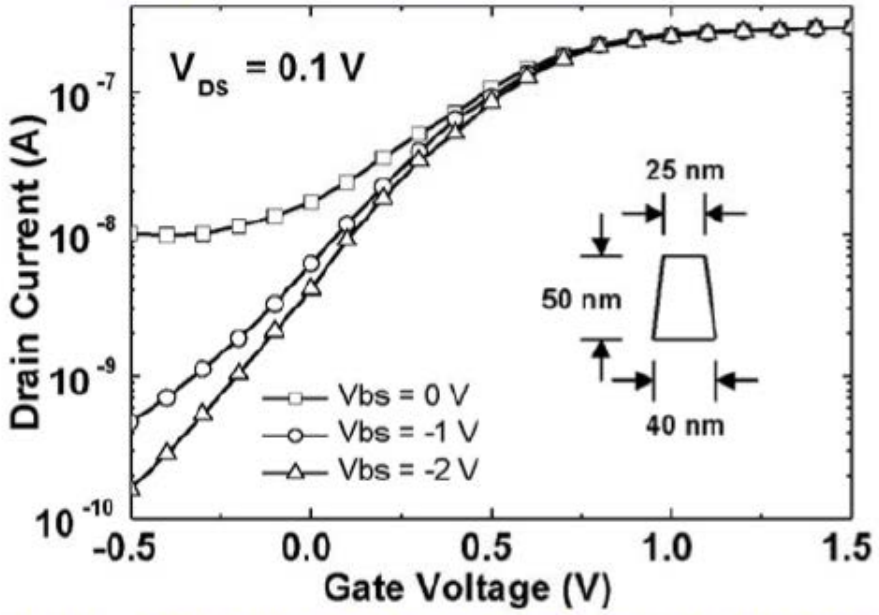
Dkt. 488, **June 11, 2018 PM Trial Tr.** at 100:20-101:2 (Prof. Lee)

Presentations Reference Lee Publications

First Bulk FinFET in the World







I_D-V_{GS} Characteristics of 40 nm bulk N FinFET

- T. Park et al., SNU/KNU, Nanomes03 2003
- T. Park et al., SNU/KNU, Physica E19, p.6, 2003

경북대학교 Jong-Ho Lee Nanosystems Lab.

2012: Invited Prof. Lee Presentation

--- Original Message ---

From : "Kim Dong-won" <timo.kim@samsung.com>

To : jhl@snu.ac.kr

Date : 2012/01/17 Tuesday am 10:16:31

Subject : Request for a lecture at Samsung regarding FinFET

Professor Lee Jong-ho;

How are you?
This is Master Kim Dong-won of Samsung Semiconductor.
How have you been doing? I think I haven't seen you since I saw you at Kyungpook University in 2009.

I am contacting you to ask you to give a lecture regarding FinFET
and I am contacting you by mail first
because the only contact information I have is Kyungpook National University and I couldn't contact you over the internet call.

Please contact me when you have time.

==========

Dong-Won Kim, Ph.D.
Master
Logic Lab / Semiconductor R&D
Samsung Electronics Co. LTD.
OFFICE : 82-31-208-1260
PCS : 82-10-7900-8236
E-MAIL : timo.kim@samsung.com

==========

2012: Invited Prof. Lee Presentation

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and I am contacting you by mail first
because the only contact information I have is Kyungpook National University an
you over the internet call.

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Master
Logic Lab / Semiconductor R&D
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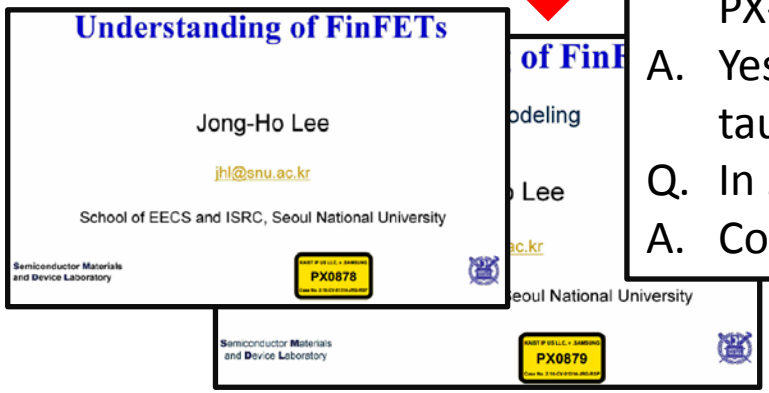
OFFICE : 82-31-208-1260
PCS : 82-10-7900-8236
E-MAIL : timo.kim@samsung.com
==========

KAIST IP US LLC, v. SAMSUNG
PX1377
Case No. 2:16-CV-01314-JRG-RSP



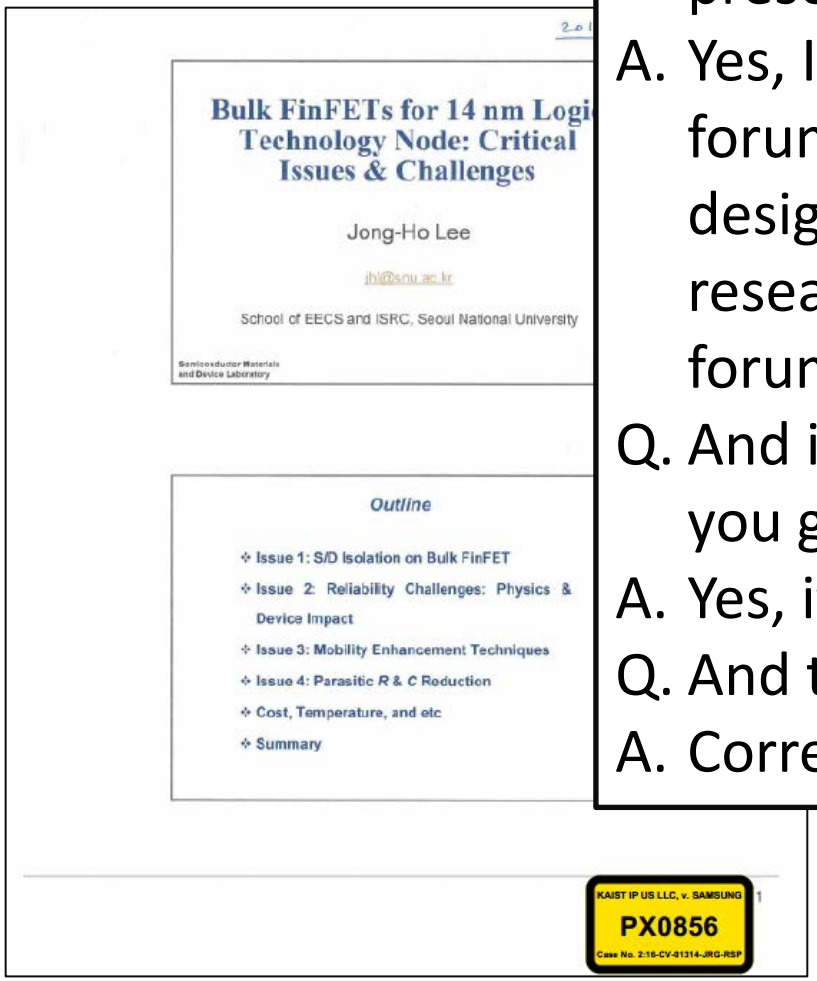
Q. Why did Samsung ask -- what did Samsung ask of you after Intel's announcement?
A. Samsung asked me to provide a multi-day lecture on bulk FinFET, and it– they wanted the lecture to solely be on bulk FinFET.
Q. Who invited you to teach Samsung's engineers?
A. Dr. Dong-Won Kim, an executive at Samsung R&D laboratory.
Q. And is PX-1377 his invitation.
A. Yes.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 102:6-15 (Prof. Lee)

Q. Now, I want to turn to PX-1377 -- excuse me, PX-878 and PX-879. Do you recognize these documents?
A. Yes. This is the presentation material that I used when I taught Samsung engineer on bulk FinFET.
Q. In 2012?
A. Correct.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 102:25-103:6 (Prof. Lee)

2012: Invited Prof. Lee Presentation



Q. Did Samsung ask you to give any other presentations after this one in 2012?

A. Yes, I was invited to lecture at the Samsung forum on 14-nanometer bulk FinFET design. Many Samsung executives and researchers participated in the Samsung forum.

Q. And is that -- is PX-856 the presentation you gave?

A. Yes, it is.

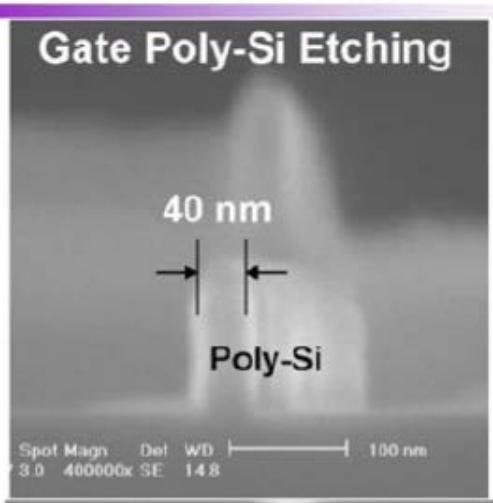
Q. And this was in 2012; is that correct?

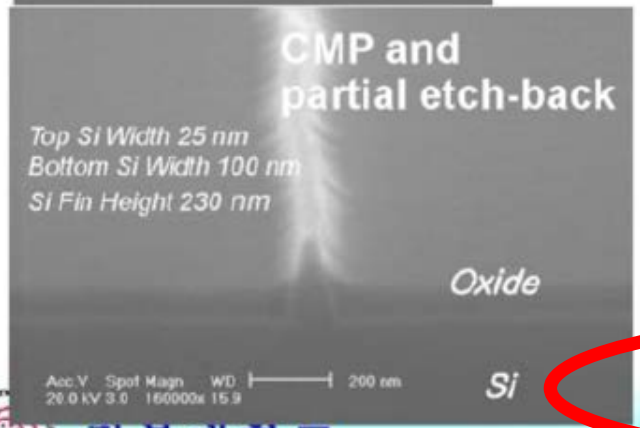
A. Correct.

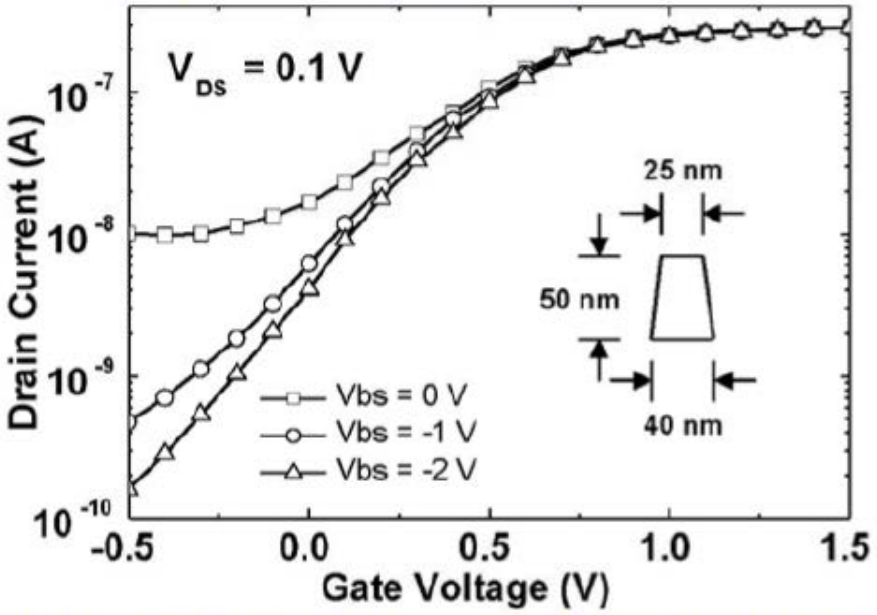
Dkt. 488, **June 11, 2018 PM Trial Tr.** at 103:16-24 (Prof. Lee)

Presentations Reference Lee Publications

First Bulk FinFET in the World







I_D-V_{GS} Characteristics of 40 nm bulk N FinFET

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경북대학교 Jong-Ho Lee Nanosystems Lab.

Presentations Reference Lee Publications

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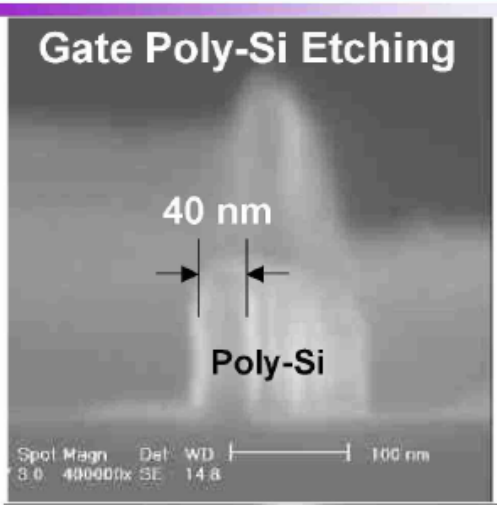

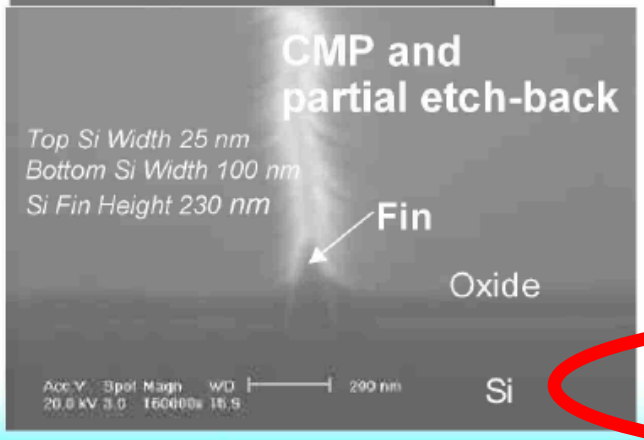

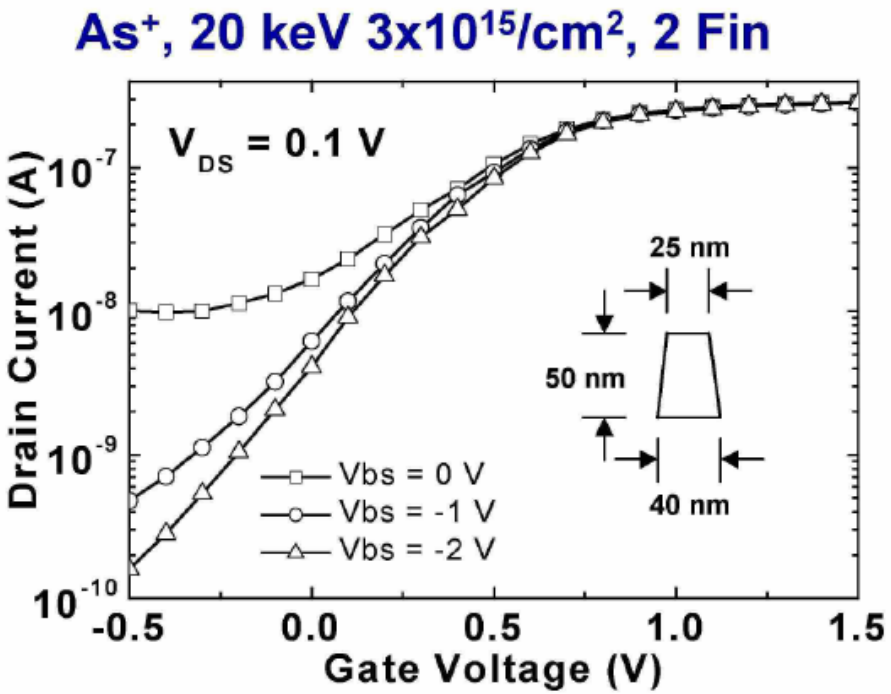

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Nanosystems Lab.

Jong-Ho Lee

SUNGPOOK NATIONAL UNIVERSITY

Presentations Refer to Patent Claims

Understanding of FinFETs

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School of EECS and ISRC, Seoul National University

Semiconductor Materials and Device Laboratory

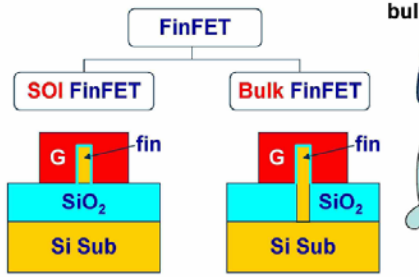
PX0878

KAIST-000385

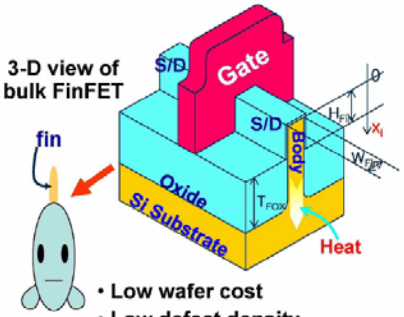
23

Bulk FinFETs (Double- or Tri-gate MOSFETs)

◆ What's bulk FinFET?



3-D view of bulk FinFET



- Low wafer cost
- Low defect density
- No floating body effect
- High heat transfer rate to substrate
- Good process compatibility

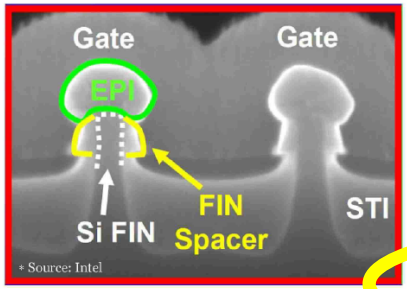
* Korea/USA patent

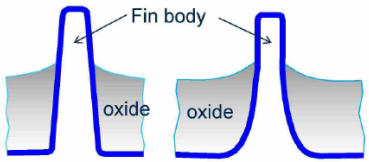
KAIST-000406

PX0878.24

61

Comparison of Fin body Shape





wherein the resistance of said Fin active region is reduced by enlarging the width of said Fin active region within the oxidat... the bulk silicon ...strate.

15. The device as claimed in claim 1, wherein the two top corners of said Fin active region are chamfered through an ...xidation and etching, or (and) annealing process in ...hydro... ...atmosphere.

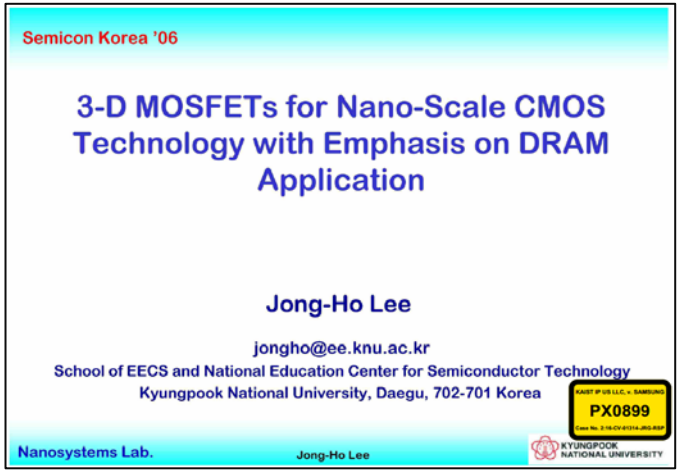
청구항 14.
청구항 1에 있어서, 상기 Fin액티브 영역의 폭이 벌크 실리콘기판에 가까워지면서 산화막 내에서 넓어져 상기 Fin액티브 영역의 저항이 줄어듬을 특징으로 하는 이중-게이트 F i n F E T 소자.

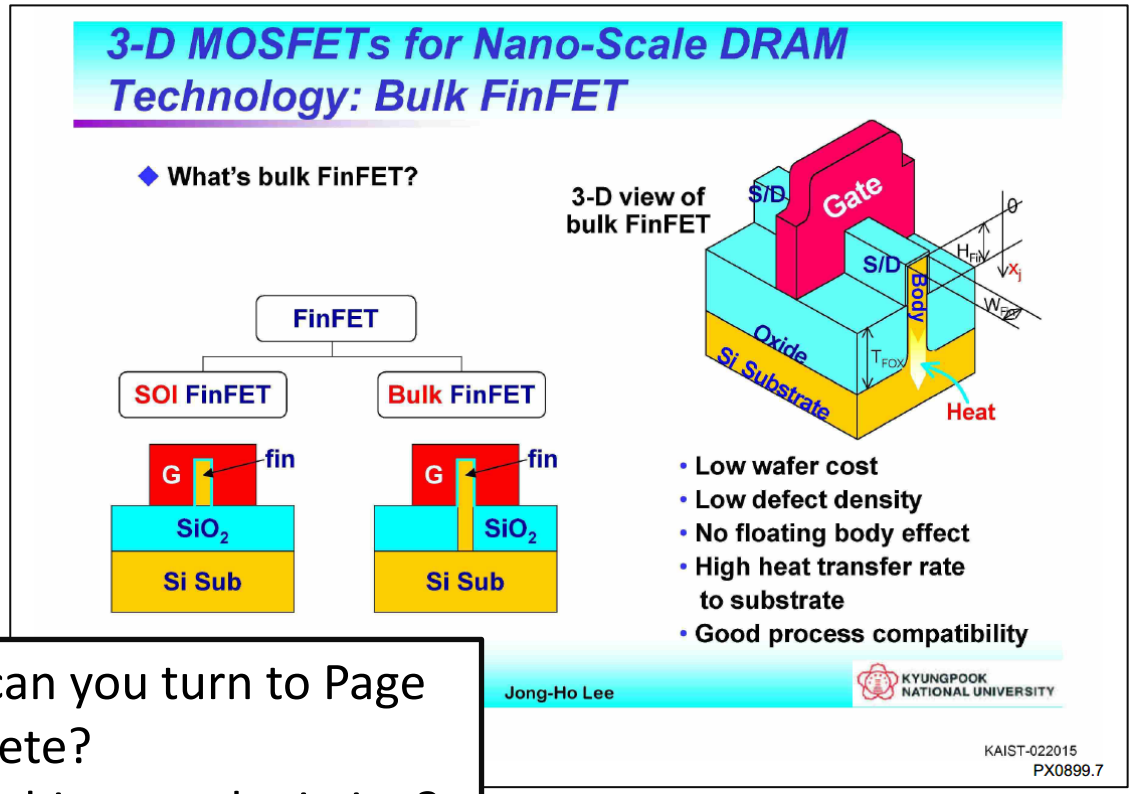
청구항 15.
청구항 1에 있어서, 상기 Fin액티브 영역이 상부 폭은 좁고, 하부 폭이 넓은 사다리꼴 모양인 것을 특징으로 하는 이중-게이트 F i n F E T 소자.

KAIST-000446

PX0878.62

Presentations Describe Patented Design





MR. SHEASBY: And can you turn to Page 7 of this document, Mr. Negrete?

Q. (By Mr. Sheasby) What is this page depicting?

A. This is explaining the general advantages of bulk FinFET over the alternative which is silicon-on-insulator FinFET.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 100:15-19 (Prof. Lee)

Presentations Describe Patented Design

Fin shape

2012

Bulk FinFETs for 14 nm Logic Technology Node: Critical Issues & Challenges

Jong-Ho Lee

jhl@snu.ac.kr

School of EECS and ISRC, Seoul National University

Semiconductor Materials and Device Laboratory

Outline

- Issue 1: S/D Isolation on Bulk FinFET
- Issue 2: Reliability Challenges: Physics & Device Impact
- Issue 3: Mobility Enhancement Techniques
- Issue 4: Parasitic *R* & *C* Reduction
- Cost, Temperature, and etc
- Summary

KAIST IP US LLC, v. SAMSUNG
PX0856
Case No. 2:16-CV-01314-JRG-RSP

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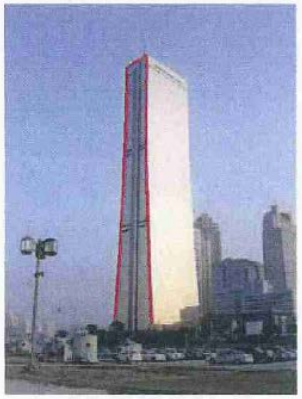
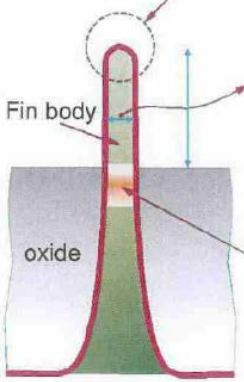
Summary on S/D Isolation of Bulk FinFET

◆ **Body Profile and Doping**



63 Building

Mechanically stable



- Rounded corner: Better reliability
- S/D $x_j \leq H_{fin}$
- Uniform body width

DIBL variation in both bulk & SOI FinFETs

EUV ? or 193i quadruple?

- Local doping

Quite similar DIBL to that of SOI FinFET

- Mechanically stable
- Body resistance reduction due to field V_t implant

Presentations Describe Patented Design

Source/Drain Junction Depth (Claims 11 and 12):

Understanding of FinFETs

Jong-Ho Lee

jhl@snu.ac.kr

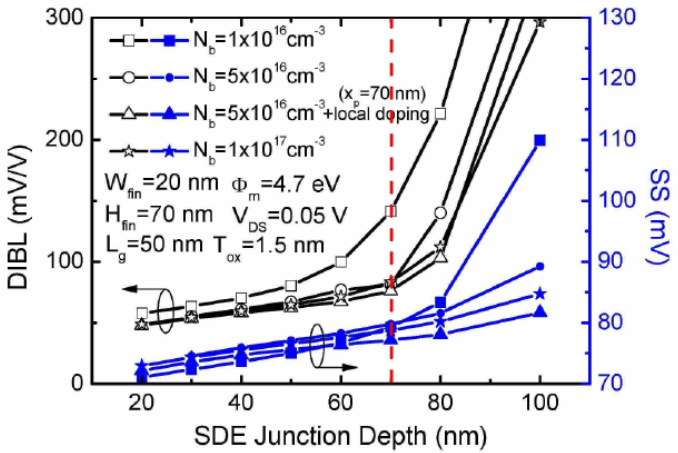
School of EECS and ISRC, Seoul National Universit

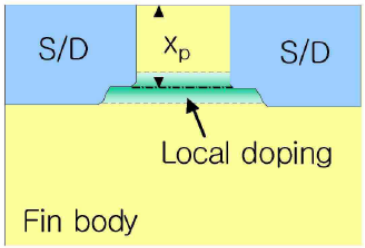
Semiconductor Materials and Device Laboratory

PX0878

42

S/D Junction Depth Design of Bulk FinFET





- Local doping
  - x_p=70 nm
  - N_{Local}=1x10^{18} cm^{-3}

- Low body doping: $x_{j,SDE} > H_{fin}$ → DIBL & SS ↓(due to bulk punch-through)
- Medium body doping: $x_{j,SDE} \cong H_{fin}$ + 10 nm
- To prevent bulk punch-through : $x_{j,SDE} \leq H_{fin}$ and/or local doping

KAIST-000427
PX0878.43

Presentations Describe Patented Design

Enlarging Fin Active Region (Claim 13):

Understanding of FinFETs

Jong-Ho Lee

jhl@snu.ac.kr

School of EECS and ISRC, Seoul National University

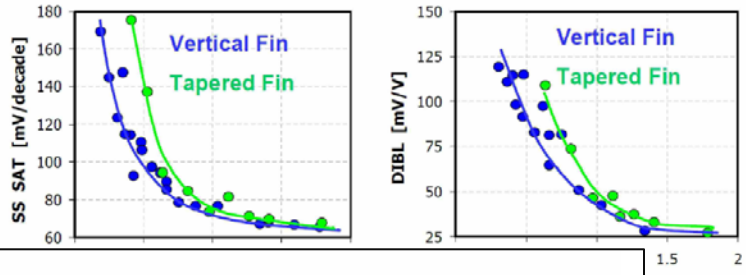
Semiconductor Materials and Device Laboratory

PX0878

KAIST-000365
PX0878.1

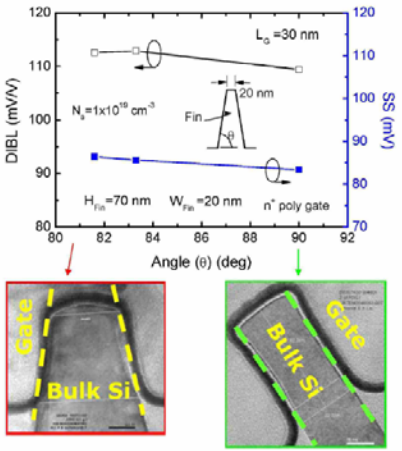
47

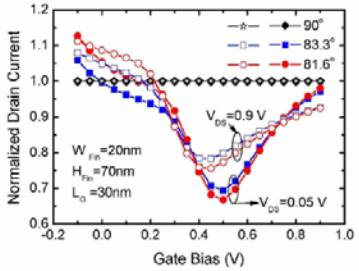
Impact of Fin Profile



46

Device Characteristics with Body Angle





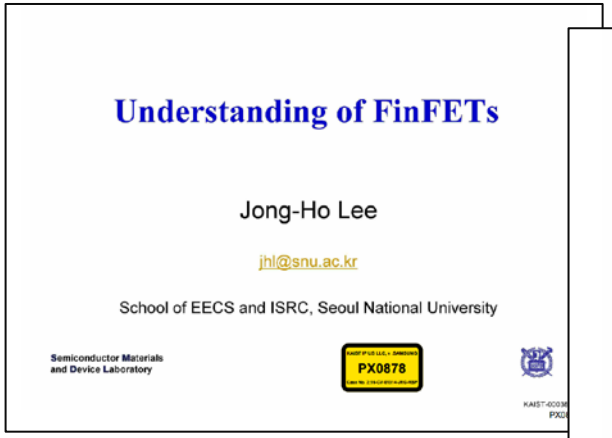
- Tapered fin widens – degraded SCEs
- Closer to 90o of body angle, better DIBL and drain current

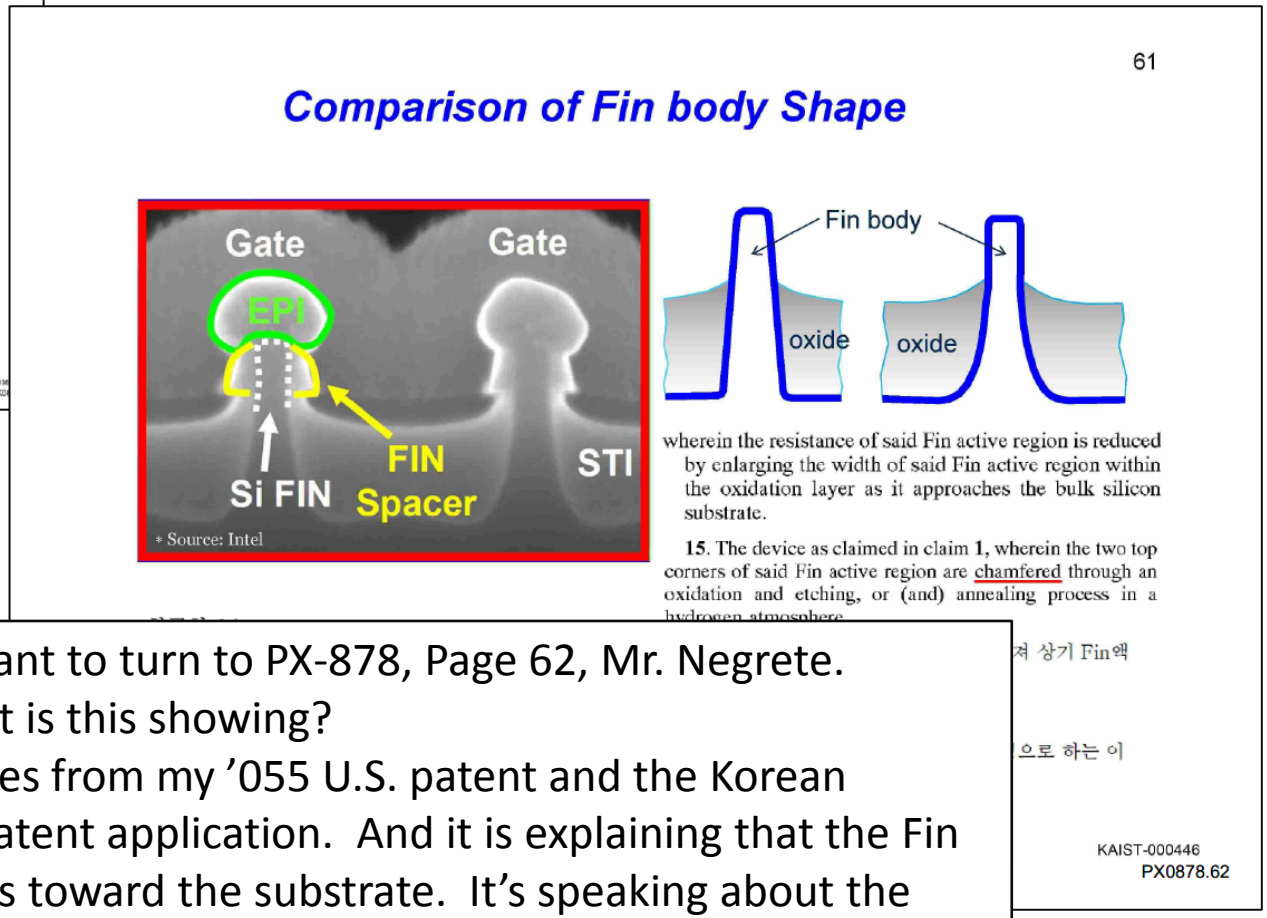
KAIST-000431
PX0878.47

KAIST-000432
PX0878.48

Presentations Describe Patented Design

Enlarging Fin (Claim 13) and Chamfering (Claim 15):





MR. SHEASBY: And I want to turn to PX-878, Page 62, Mr. Negrete.

Q. (By Mr. Sheasby) What is this showing?

A. This is showing passages from my '055 U.S. patent and the Korean counterpart, Korean patent application. And it is explaining that the Fin should widen as it goes toward the substrate. It's speaking about the importance of that. And also, it is showing techniques of chamfering, in other words, rounding the top corners of the Fin.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 103:7-15 (Prof. Lee)

Presentations Describe Patented Design

Wall-shape (All Claims) and Enlarging Fin (Claim 13):

삼성전자 세미나 2006.1

Bulk FinFETs for DRAM Application

KAIST IP US LLC, v. SAMSUNG
PX1608
Case No. 2:16-CV-01314-JRG-RSP

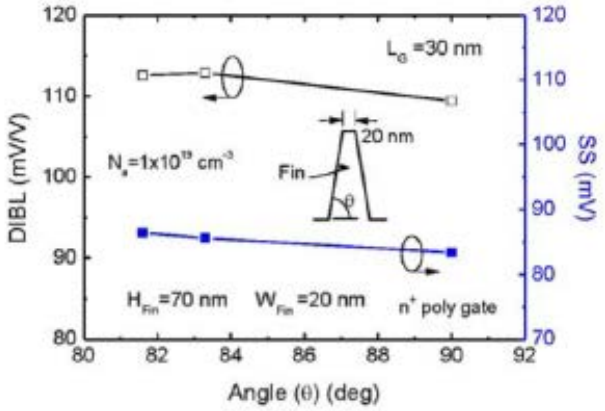
Jong-Ho Lee

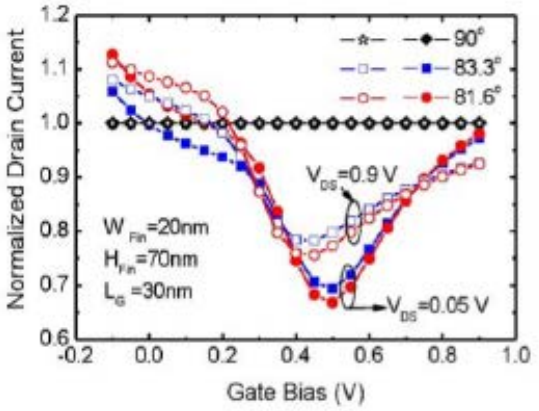
jongho@ee.knu.ac.kr

School of EECS and National Education Center for Semiconductor Techno
Kyungpook National University, Daegu, *702-701 Korea*

경북대학교 Jong-Ho Lee Nanosys

Device Characteristics with Body Angle



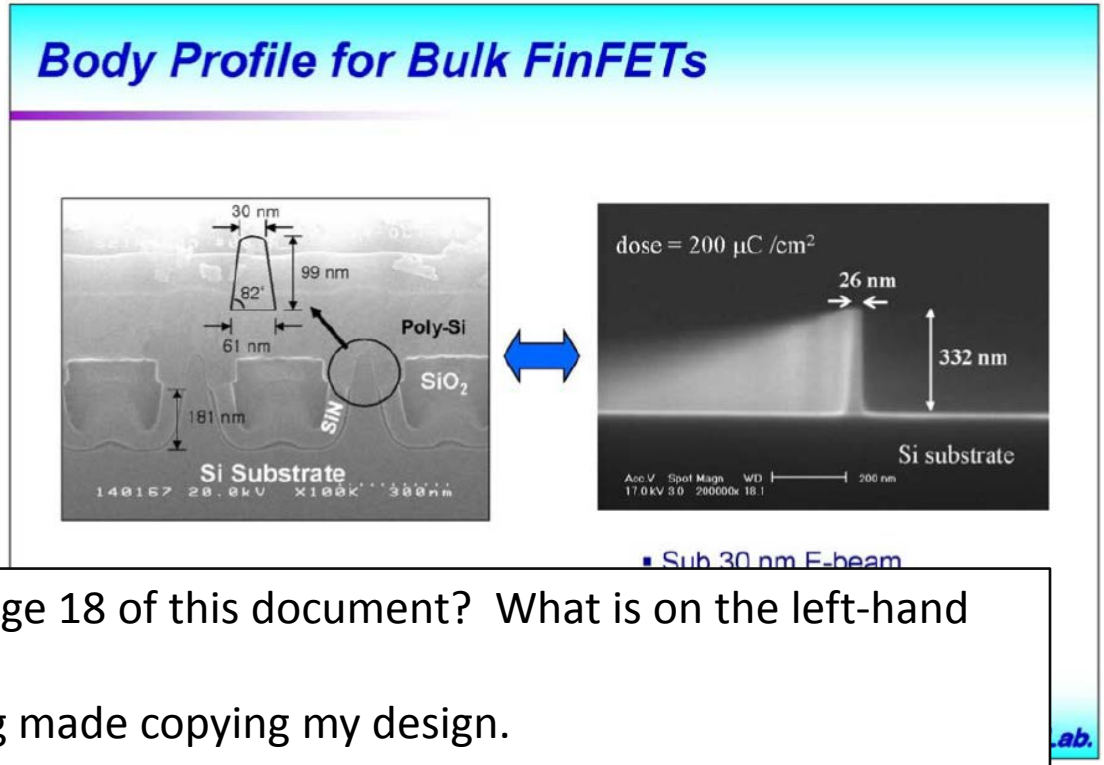


- Closer to 90° of body angle, better DIBL and drain current

경북대학교 Jong-Ho Lee Nanosystems Lab.

Presentations Describe Patented Design

Wall-shape (All Claims) and Enlarging Fin (Claim 13):



Q. All right. Can you turn to Page 18 of this document? What is on the left-hand side of this document?

A. This is the Fin that Samsung made copying my design.

…

Q. What is the right-hand side, Professor?

A. The right-hand side is the Fin that was made at our laboratory under my direction. The Fin is more advanced. It's taller and thinner, and the Fin body widens as it goes toward the substrate.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 101:3-12 (Prof. Lee)

Presentations Describe Patented Design

Nonoverlapping Gate (All Claims):

삼성전자 세미나 2006.1

Bulk FinFETs for DRAM Application

Jong-Ho Lee

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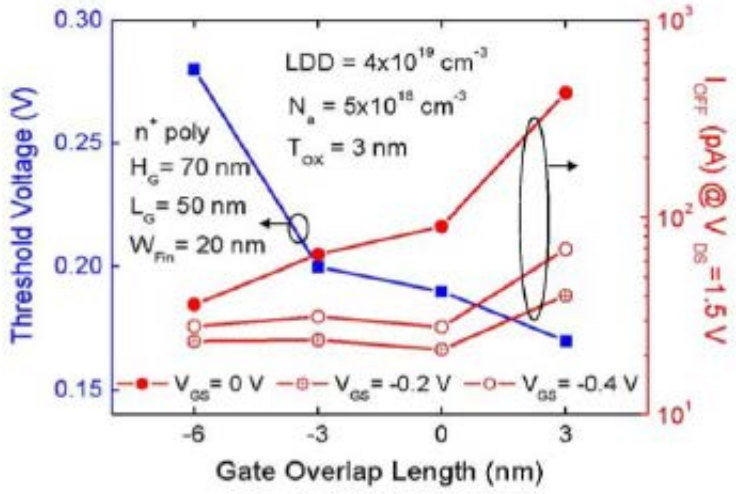
경북대학교 *Jong-Ho Lee* Nan

KAIST IP US LLC, v. SAMSUNG
PX1608
Case No. 2:16-CV-01314-JRG-RSP

V_T and I_{OFF} Char. wrt. Gate Overlap Length



- 0 to –3 nm overlap is reasonable

경북대학교 *Jong-Ho Lee* **Nanosystems Lab.**

Samsung Did Not Independently Design

D.W. Kim's conclusory testimony:

"[W]hen I look at the technology of our 14-nanometer products and based on that when I look at the ['055] patent, there was no relevance whatsoever."

Dkt. 493 (6/13/18 AM), at 111:2-5.

CONTRADICTED BY:

Former Samsung engineer Tai-Su Park admitted that he took Prof. Lee's designs and presented them to Samsung.

Dkt. 494 (6/13/18 PM), at 40:20-41:1

D.W. Kim admitted that he reviewed Prof. Lee's publications when he began working on commercial FinFET designs at Samsung.

Dkt. 494 (6/13/18 PM), at 4:24-5:2

Samsung engineers repeatedly accessed Prof. Lee's research throughout the development process.

Dkt. 488 (6/11/18 PM), at 100:2-10, 100:20-101:2, 102:6-15, 103:16-24
PX1375; PX1377

Jury Properly Found No Good Faith

Evidence: No Investigation

QUESTION: Did Samsung every provide a technical explanation as to why it did not infringe the ’055 patent?

ANSWER: Although I cannot give you a very definitive answer to that, with respect to infringement or not, in order to tell that there are - - that a certain patent is infringed or not, we would have to explain our products, but that would be a confidential information. So I think we would not have given a very specific answer to that effect. For example, this is not infringed because of this and this and that. We would not have given such answers.

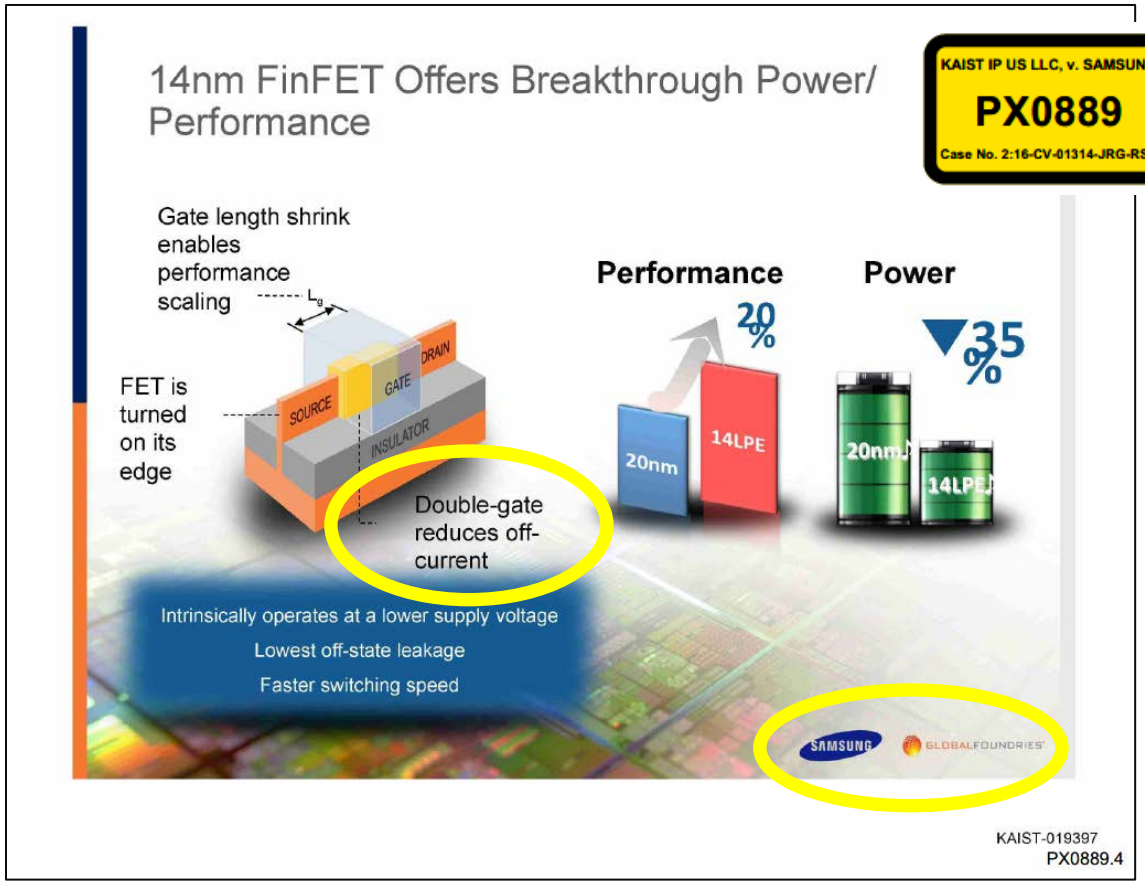
Dkt. 493, **June 13, 2018 AM Trial Tr.** at 67:3-13 (Jong-soo Seo)

Dongwon Kim's Trial Testimony Contradicted

Samsung noninfringement argument:

→ *Not a double-gate*

CONTRADICTED by Samsung Own Documents



Dongwon Kim's Trial Testimony Contradicted

Samsung noninfringement argument:

→ *No wall-shape Fin*

CONTRADICTED by: **Samsung engineer Heedon Jeong**

QUESTION: Now, the Fin active region in the 14-nanometer devices is on the surface of the bulk silicon substrate, correct?
ANSWER: Yes.
QUESTION: It's a wall-shape single crystalline silicon?
ANSWER: Yes, that's a single crystalline.
QUESTION: The answer to my question is yes, then?
ANSWER: Yes.

Dkt. 493, June 13, 2018 AM Trial Tr. at 47:21-48:4

Dongwon Kim's Trial Testimony Contradicted

Samsung noninfringement argument:

→ *No separate first oxide layer, it is only one continuous layer*

CONTRADICTED by:

Dr. Subramanian testified the opposite

Q. In fact, the specification describes the first oxide layer and gate oxide layer as different regions of one continuous layer that surrounds the Fin active region, fair?

A. Yes, generally that's a fair description.

Q. Is it -- is it a fair description, yes or no?

A. Yes, I think so.

Dkt. 496, **June 14, 2018 AM Trial Tr.** at 86:15-20 (cross)

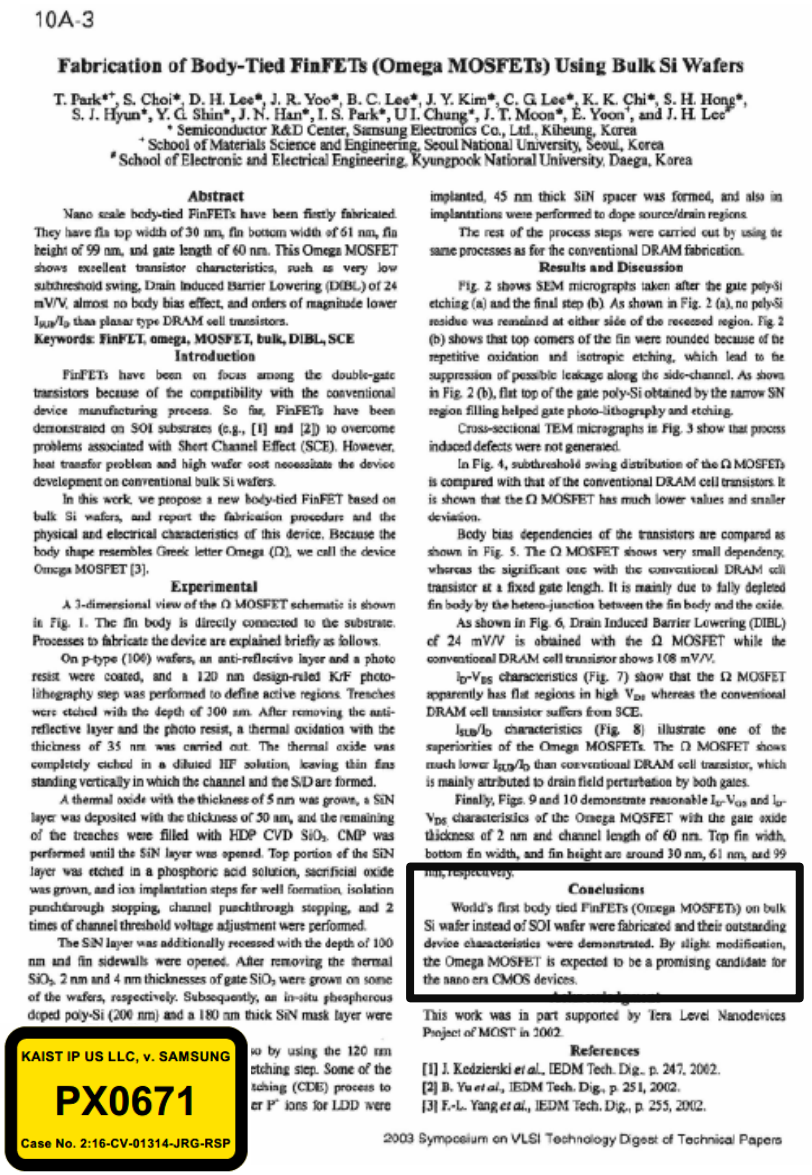
Samsung engineer Heedon Jeong testified the opposite

Q. And so just like in that figure, it's depicting one continuous - - continuous oxide layer on all three sides of the Fin, correct?

A. Correct.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 43:9-12

Samsung Endorsed Novelty



10A-3

Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers

T. Park*†, S. Choi*, D. H. Lee*, J. R. Yoo*, B. C. Lee*, J. Y. Kim*, C. G. Lee*, K. K. Chi*, S. H. Hong*, S. J. Hyun*, Y. G. Shin*, J. N. Han*, I. S. Park*, U I. Chung*, J. T. Moon*, E. Yoon†, and J. H. Lee‡
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‡ School of Electronic and Electrical Engineering, Kyungpook National University, Daegu, Korea

Abstract

Nano scale body-tied FinFETs have been firstly fabricated. They have fin top width of 30 nm, fin bottom width of 61 nm, fin height of 99 nm, and gate length of 60 nm. This Omega MOSFET shows excellent transistor characteristics, such as very low subthreshold swing, Drain Induced Barrier Lowering (DIBL) of 24 mV/V, almost no body bias effect, and orders of magnitude lower I_{GIDL}/I_D than planar type DRAM cell transistors.

Keywords: FinFET, omega, MOSFET, bulk, DIBL, SCE

Introduction

FinFETs have been on focus among the double-gate transistors because of the compatibility with the conventional device manufacturing process. So far, FinFETs have been demonstrated on SOI substrates (e.g., [1] and [2]) to overcome problems associated with Short Channel Effect (SCE). However, heat transfer problem and high wafer cost necessitate the device development on conventional bulk Si wafers.

In this work, we propose a new body-tied FinFET based on bulk Si wafers, and report the fabrication procedure and the physical and electrical characteristics of this device. Because the body shape resembles Greek letter Omega (Ω), we call the device Omega MOSFET [3].

Experimental

A 3-dimensional view of the Ω MOSFET schematic is shown in Fig. 1. The fin body is directly connected to the substrate. Processes to fabricate the device are explained briefly as follows.

On p-type (100) wafers, an anti-reflective layer and a photo resist were coated, and a 120 nm design-ruled KrF photo-lithography step was performed to define active regions. Trenches were etched with the depth of 300 nm. After removing the anti-reflective layer and the photo resist, a thermal oxidation with the thickness of 35 nm was carried out. The thermal oxide was completely etched in a diluted HF solution, leaving thin fins standing vertically in which the channel and the S/D are formed.

A thermal oxide with the thickness of 5 nm was grown, a SiN layer was deposited with the thickness of 50 nm, and the remaining of the trenches were filled with HDP CVD SiO_2. CMP was performed until the SiN layer was opened. Top portion of the SiN layer was etched in a phosphoric acid solution, sacrificial oxide was grown, and ion implantation steps for well formation, isolation punchthrough stopping, channel punchthrough stopping, and 2 times of channel threshold voltage adjustment were performed.

The SiN layer was additionally recessed with the depth of 100 nm and fin sidewalls were opened. After removing the thermal SiO_2, 2 nm and 4 nm thicknesses of gate SiO_2 were grown on some of the wafers, respectively. Subsequently, an in-situ phosphorous doped poly-Si (200 nm) and a 180 nm thick SiN mask layer were

so by using the 120 nm
etching step. Some of the
tching (CDE) process to
er P^+ ions for LDD were

implanted, 45 nm thick SiN spacer was formed, and also ion implantations were performed to dope source/drain regions.

The rest of the process steps were carried out by using the same processes as for the conventional DRAM fabrication.

Results and Discussion

Fig. 2 shows SEM micrographs taken after the gate poly-Si etching (a) and the final step (b). As shown in Fig. 2 (a), no poly-Si residue was remained at either side of the recessed region. Fig. 2 (b) shows that top corners of the fin were rounded because of the repetitive oxidation and isotropic etching, which lead to the suppression of possible leakage along the side-channel. As shown in Fig. 2 (b), flat top of the gate poly-Si obtained by the narrow SiN region filling helped gate photo-lithography and etching.

Cross-sectional TEM micrographs in Fig. 3 show that process induced defects were not generated.

In Fig. 4, subthreshold swing distribution of the Ω MOSFETs is compared with that of the conventional DRAM cell transistors. It is shown that the Ω MOSFET has much lower values and smaller deviation.

Body bias dependencies of the transistors are compared as shown in Fig. 5. The Ω MOSFET shows very small dependency, whereas the significant one with the conventional DRAM cell transistor at a fixed gate length. It is mainly due to fully depleted fin body by the hetero-junction between the fin body and the oxide.

As shown in Fig. 6, Drain Induced Barrier Lowering (DIBL) of 24 mV/V is obtained with the Ω MOSFET while the conventional DRAM cell transistor shows 108 mV/V.

I_D-V_{DS} characteristics (Fig. 7) show that the Ω MOSFET apparently has flat regions in high V_{DS} whereas the conventional DRAM cell transistor suffers from SCE.

I_{GIDL}/I_D characteristics (Fig. 8) illustrate one of the superiorities of the Omega MOSFETs. The Ω MOSFET shows much lower I_{GIDL}/I_D than conventional DRAM cell transistor, which is mainly attributed to drain field perturbation by both gates.

Finally, Figs. 9 and 10 demonstrate reasonable I_D-V_{GS} and I_D-V_{DS} characteristics of the Omega MOSFET with the gate oxide thickness of 2 nm and channel length of 60 nm. Top fin width, bottom fin width, and fin height are around 30 nm, 61 nm, and 99 nm, respectively.

Conclusions

World's first body tied FinFETs (Omega MOSFETs) on bulk Si wafer instead of SOI wafer were fabricated and their outstanding device characteristics were demonstrated. By slight modification, the Omega MOSFET is expected to be a promising candidate for the nano era CMOS devices.

This work was in part supported by Tera Level Nanodevices Project of MOST in 2002.

References

[1] J. Kedzierski *et al.*, IEDM Tech. Dig., p. 247, 2002.
[2] B. Yu *et al.*, IEDM Tech. Dig., p. 251, 2002.
[3] F.-L. Yang *et al.*, IEDM Tech. Dig., p. 255, 2002.

"World's first body tied FinFETs (Omega MOSFETs) on bulk Si wafer instead of SOI wafer were fabricated and their outstanding device characteristics were demonstrated."

PX0671 (Tai-Su Park, et al., *Fabrication of Body-Tied FinFETs (Omega MOSFETs) Using Bulk Si Wafers*, 2003 SYMP. VLSI TECH. DIG. 135).

Recklessness

Top Samsung Execs Given Opportunity To License

2002 email from Samsung VP Dr. Dong-gun Park to Prof. Lee:

"… we cannot unreasonably pursue what this company cannot do. I think it is my mission to find the most effective way to make profit in the future with a certain budget and to promote technology and to implement it."

PX1374

2002 email from Samsung CEO Dr. Kinam Kim to Prof. Lee:

"And, as to the patent of double gate that you are doing, it is difficult to do the project at this time."

PX2068

Evidence: Discussions w/ Samsung

Q. Did you interact with any Samsung executives regarding your bulk FinFET invention?

A. I interacted with Samsung R&D group senior executives, two were Dr. Kinam Kim and Dr. Donggun Park.

Q. What were your interactions with Kinam Kim?

A. I spoke about bulk -- bulk FinFET with him, I told him that I had filed a Korean patent, which is the same as the ’055 patent, and I urged him to collaborate further in research, and I told him to license the technology.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 97:5-13 (Lee)

Evidence: Discussions w/ Samsung

Q. Can you turn to PX-2068? Do you recognize this document?
A. This is an e-mail from Dr. Kinam Kim.
Q. I want to direct your attention to the language at the end. "As to the patent on double-gate that you are doing." Do you know what patent he was referring to?
A. This is referring to the Korean patent application which is the same as the '055 U.S. patent.

Dkt. 488, **June 11, 2018 PM Trial Tr.** at 97:14-21 (Prof. Lee)

Evidence: Kinam Kim emails

-----Original Message-----
From: kkn0414@samsung.co.kr [mailto:kkn0414@samsung.co.kr]
Sent: Monday, April 1, 2002 9:50 AM
To: jongho@ee.knu.ac.kr
Subject: (Repy) Greetings and Inquiry

a convenient time, please send it to me. Let me check.
And, as to the patent of double gate that you are doing, it is difficult to do the project at this time. The projects beginning this year have been evaluated already, so it might be possible to start anew only next year. I think it is good to discuss it again then.

Have a nice week.

Best wishes

Kinam Kim

And, as to the patent of double gate that you are doing, it is difficult to do the project at this time. The projects beginning this year have been evaluated already, so it might be possible to start anew only next year. I think it is good to discuss it again then.

[page number]

KAIST IP US LLC, v. SAMSUNG
PX2068
Case No. 2:16-CV-01314-JRG-RSP

Evidence: Dongun Park emails

-----Original Message-----

-----Original Message-----
From: dgpark1@samsung.co.kr [mailto:dgpark1@samsung.co.kr]
Sent: Monday, November 25, 2002 1:13 PM
To: jongho@ee.knu.ac.kr
Subject: (Reply) Inquiry

company cannot do. I think it is my mission to find the most effective way to make profit in the future with a certain budget and to promote technology and to implement it.

Body Tied Fin FET is a structure that I myself thought about a lot while discussing with DIgh Hisamoto while at Berkeley.
Of course, because I returned home right away, put in charge of DRAM development, I made no real progress.
Of course, I don't have any desire to dispute your position, Professor Lee, on your prior development.

resource problems from the schedule that I originally planned.
At this time, a senior engineer happened to be there, so I thought it would be good to assign the work to Senior engineer Park. Of course I overlooked his status as student, and I think this part was my mistake.
I am sorry and I plan to proceed the work independently from now on.
Such a part is the difficulty in the work called joint development.

I am sorry about the patent, but I have never offered any opinion on it, and I think I made my it clear at the last meeting that the patent is not ours as our company did not develop it.
I still don't understand why this issue keeps coming up.
Can't you just register the patent? I don't understand what you are saying at all.

Can't you just register the patent? I don't understand what you are saying at all.

I don't understand why I have to write such a mail spending time like this, but I am sor

[page number]

KAIST IP US LLC, v. SAMSUNG
PX1374
Case No. 2:16-CV-01314-JRG-RSP

Concealment by D.W. Kim

Q. When did you next speak with him after that?

A. That was after my promotion to the position of master, which was in December 2011. And we masters would have -- have the responsibility of providing training to our members. So I invited Professor Jong-Ho Lee to provide a lecture to our junior engineers on that occasion.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 104:15-20 (Dongwon Kim)

Q. Was there something happening in 2012 that made it of interest for you to have somebody come in an speak with junior engineers relating to FinFET technology?

A. That's right. That was when we had just provided our PDKs [process design kits] to our customers in -- in December of 2012, right. So we needed lot of engineers to be familiar with the technology for the purposes of 14-nanometer mass production. So the -- the title of the lecture was understanding of FinFET technology.

Dkt. 493, **June 13, 2018 AM Trial Tr.** at 105:7-13 (Dongwon Kim)

Evidence: Still In Development

Q. The shape of the selective epitaxial source/drain layers in the 14-nanometer LPE process was defined in 2011, 2012, and 2013, correct?

A. It was defined in 2011, and it is something that is subject to change based upon request by customers.

Q. So when I read from your deposition, Volume 1, 154, 19 through 23.

> Question: When did you define this - - when do you define the shape of the selective epitaxial source/drain layers in the 14-nanometer LPE process?
> Answer: It is defined - - it was defined over the time period of 2011, 2012, and 2013.

Did I read your testimony correctly?

A. Yes, you did.

Dkt. 494, **June 13, 2018 PM Trial Tr.** at 7:17-8:8 (Dongwon Kim cross)

Evidence: Still in development

Q. So when I read from your deposition, Volume 1, 154, 19 through 23.

Question: When did you define this - - when do you define the shape of the selective epitaxial source/drain layers in the 14-nanometer LPE process?

Answer: It is defined - - it was defined over the time period of 2011, 2012, and 2013.

Did I read your testimony correctly?

A. Yes, you did.

Dkt. 494, June 13, 2018 PM Trial Tr. at 7:17-8:5 (Dongwon Kim cross)

QUESTION: So the commercial 14-nanometer LPE bulk FinFET design was released to manufacturing some time between 2013 and 2014, correct?

ANSWER: Correct.

Dkt. 493, June 13, 2018 AM Trial Tr. at 48:20-23 (Heedon Jeong)

Evidence: Date of Infringement

Q. And the hypothetical negotiations with each Defendant in this case would have occurred in late 2015 or early 2015, right?

A. That's -- that's fair, yes, sir.

Dkt. 491, **June 12, 2018 PM Trial Tr.** at 212:25-213:3 (Weinstein cross)

Q. The hypothetical negotiation in this case occurs in early 2015, fair?

A. I think late '14 and early '15, yes.

Dkt. 497, **June 14, 2018 PM Trial Tr.** At 108:14-16 (Becker cross)

Accused Product Still in Development

Samsung argues:

D.W. Kim said no copying because "in January 2012, we had already provided our PDKs [process design kits] to our customers, so what that means is the production definition was all completed by then."

Dkt. 493 (6/13/18 AM) at 106:9-11.

CONTRADICTED BY:

Dongwon Kim admitting 14LPE still being defined through 2013

Dkt. 494 (6/13/18 PM), at 7:17-8:8

Heedon Jeong admitting 14LPE design not released to manufacturing until 2013-2014

Dkt. 493 (6/13/18 AM), at 48:20-23

Samsung admission: "the period of 2011-2013 when Samsung developed the Accused Products."

Dkt. 607 at 12

No Judicial Estoppel

No Judicial Estoppel

Samsung ***never relied*** on <u>any promise or implied grant</u>

> "The Court concludes that Samsung's decision to proceed with a commercial bulk FinFET transistor was not premised in any way on a reasonable belief that Defendants had rights to use the '055 Patent, or that the '055 Patent would not be asserted against it."

Dkt. 574, CL39

BUT THERE IS EVIDENCE that <u>Samsung's engineers copied</u>

Defendants Ignore Last Sentence

[FF152] "Based on the record before the Court, the Court finds that Defendants have not proven that Samsung relied on the '055 Patent or Professor Lee's statements regarding the patent technology of the 055 Patent ***when it decided to commercialize the 14nm bulk FinFET technology.***"

Dkt. 574, FF27

Court Found That There Was Decision Not To Design Around

[CL40] "Defendants ***declined to make non-infringing design changes to the bulk FinFET transistor*** even after P&IB approached them about licensing the patent, despite the fact that there was an opportunity to influence the shape of the source and drain regions of the device."

Dkt. 574

KAIST Argued No Consideration By Decisionmakers

103. Dongwon Kim did not make the decision to commercialize a bulk FinFET transistor. He testified that the decision was made by the head of the R&D center, Jung Chilhee, in 2010. Dkt. 547-9 (D. Kim Dep. Tr., Vol. 1), at 31:25-32:23.

103. Neither ***Dongwon Kim, nor any other witness for Defendants, provided any admissible evidence regarding the mental state of the individuals who made the decision to launch the bulk FinFET design in the U.S., their views of Professor Lee's interactions with Samsung, or their views of the '055 Patent***. June 13, 2013 P.M. Trial Tr. 6:2-15 (Dongwon Kim testifying that he worked under Donggun Park and Kinam Kim but did not collect information from them in preparation for testimony). Dkt. 549.

Dkt. 569

Defendants Misquote KAIST Filings

Samsung's Willfulness JMOL, at 4

"Plaintiff then proposed that the Court find as fact that Samsung "did not consider the '055 Patent when developing the infringing technology," that Professor Lee's presentations "did not influence [Samsung] to develop the 14 nm bulk FinFET design," and that Samsung's "decision makers" likewise did not consider the patent in deciding to "launch the bulk FinFET design in the U.S." Dkt. 569 ¶¶ 95, 99, 101, 104-05."

KAIST's Proposed Findings (Dkt. 569)

99. Dongwon Kim testified that he did not consider the '055 Patent when developing the infringing technology. Dkt. 547-10 (D. Kim Dep. Tr., Vol. 2), at 314:13-20.

101. Dongwon Kim testified that the 2006 and 2012 presentations prepared by Professor Lee did not influence him to develop the 14 nm bulk FinFET design, much less that it led him to believe that Samsung had rights to the '055 Patent, or that the '055 Patent would not be asserted against Samsung . . . .

Dongwon Kim Does Not Have Personal Knowledge

31. Dongwon Kim does not state that he has any personal knowledge of this research and, by his own admission, he did not begin working on bulk FinFET until 2003. Dkt. 534-1 (Kim Decl.) ¶ 2.

Dkt. 569 (KAIST Proposed Findings of Fact and Law)

KAIST Proposed Findings Of Fact Expressly Allege Pre-Design Knowledge

64. The '055 Patent requires that there be no overlap between the source/drain and gate regions. There is no evidence that Dongwon Kim attempted to design around the '055 Patent by adjusting the shape of the source/drain regions, despite (a) becoming aware of the '055 Patent in 2012 (Dkt. 547-10 (D. Kim Dep. Tr., Vol. 2), at 316:20-25); and (b) reviewing a presentation Professor Lee gave to Samsung in 2012 that included claims from the '055 Patent (Dkt. 547-44 (PX0878), at 62 (KAIST-000446); Dkt. 547-10 (D. Kim Dep. Tr., Vol. 2), at 175:9-18, 270:16-21, 274:5-18, 287:6-11).

Dkt. 569 (KAIST Proposed Findings of Fact and Law)

KAIST Proposed Findings Of Fact Expressly Allege Copying

10. Tai-Su Park testified that he became aware of the Korean Counterpart Patent application to the '055 Patent in September 2002, and became aware of the '055 Patent in 2011. June 13, 2018 P.M. Trial Tr. 41:10-12, 43:1-4.

11. Based on the foregoing, this Court finds that Tai-Su park was informed of the existence of the Korean Counterpart Patent and the '055 Patent.

12. Tai-Su Park admitted discussing Professor Lee with Samsung's attorneys before this lawsuit. June 13, 2018 P.M. Trial Tr. 43:13-44:12.

Dkt. 569 (KAIST Proposed Findings of Fact and Law

KAIST Proposed Findings Of Fact Expressly Allege Pre-Design Knowledge

47. Professor Lee testified that, in 2002, he told Kinam Kim, the head of Samsung's relevant R&D group at the time, and now the CEO of all Samsung semiconductor business, "to collaborate further in research, and I told him to license the technology." June 11, 2018 P.M. Tr. 97:5-13.

48. This testimony is corroborated by Kinam Kim's contemporaneous email to Professor Lee, which refers to "the patent on double gate that you are doing." Dkt. 547-51 (PX2068), at 1. This is a reference to the invention in the '055 Patent. *See, e.g.*, June 11, 2018 P.M. Trial Tr. 97:17-21 (J.H. Lee).

Dkt. 569 (KAIST Proposed Findings of Fact and Law

KAIST Proposed Findings Of Fact Expressly Allege Pre-Design Knowledge

53. Defendants indicate that, in 2011, before Samsung had even made its first working test chip with the 14 nm bulk FinFET transistor, *see* FF 61, P&IB (the predecessor of KAIST IP US) notified Samsung that it "would need a license to the '055 Patent." Dkt. 534-1 (Kim Decl.) ¶ 12 ("Prof. Lee did not notify Samsung that ***he believed Samsung would need a license to the '055 Patent*** (or the Korean counterpart patent) ***until 2011, through his licensing partner P&IB***."); Dkt. 547-50 (PX1861) (communication regarding need to obtain rights in the '055 Patent sent to Samsung on Nov. 27, 2011).

Dkt. 569 (KAIST Proposed Findings of Fact and Law

Patent is Valid & Infringed Regardless of PTO Proceedings

"[C]ulpability is generally measured against the knowledge of the actor at the time of the challenged conduct."

Halo Elecs., Inc. v. Pulse Elecs., Inc., 136 S. Ct. 1923, 1933 (2016).

"[A] certificate canceling any claim of the patent finally determined to be unpatentable" will issue only "when the time for appeal has expired or any appeal proceeding has terminated."

35 U.S.C. § 307.

Continued Infringement is Willful

"The court rejects the contention that the [defendants'] continued infringement is not willful merely because the asserted claims of the patents-in-suit have been rejected in a pending reexamination. Unless and until the jury's verdict is nullified by reversal of this court's judgment on appeal, or the reexamination rejections have become final, the [defendants] are adjudged infringers."

Affinity Labs of Texas, LLC v. BMW N. Am., LLC, 783 F. Supp. 2d 891, 902 (E.D. Tex. 2011)

No Good Faith Defenses

Samsung invalidity argument:

→ *Mizuno and Hieda*

CONTRADICTED by:

Presuit – Samsung asserted Mizuno, Hieda, Inaba during licensing talks with P&IB

Dkt. 607-3

Did not show element by element analysis

Juicy Whip, Inc. v. Orange Bang, Inc., 292 F.3d 728, 738 (Fed. Cir. 2002)

And PTAB rejected all four IPR petitions based on Mizuno, Hieda and Inaba because there was ***no reasonable likelihood*** that Samsung could prevail

Dkts. 79-1, 79-2, 443-1, 443-2

Samsung VP Dong-gun Park acknowledged Prof. Lee was first to develop and invent bulk FinFET

Dkt. 488, June 11, 2018 PM Trial Tr. at 98:25-99:15 (Prof. Lee)